Audio Codec ’97

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Intel Corporation

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- Two standard packages: 48-pins and 64-pins
  AC '97 2.0 redefined the 64-pin to be entirely vendor specific
- Split digital/analog architecture for improved S/N ratio (> 90 dB achievable)
- 16-bit stereo full-duplex Codec with fixed 48K sampling rate,
  AC '97 2.0 Appendix A defines variable sample rate support up to 96 kHz
- Four analog line-level stereo inputs for connection from LINE IN, CD, VIDEO and AUX
  AC '97 2.1 Appendix D defines optional VIDEO and AUX elimination
- Two analog line-level mono inputs for speakerphone (or DLP[1]) and PC BEEP
  AC '97 2.1 Appendix D defines optional PHONE and PC_BEEP elimination
- Mono mic input switchable from two external sources
  AC '97 2.1 Appendix D defines optional MIC2
- High quality pseudo-differential CD input
- Stereo line level output
- Mono output for speakerphone (or DLP[1])
  AC '97 2.1 Appendix D defines optional MONO_OUT elimination
- Power management support
- Optional tone control
- Optional loudness control
- Optional 3D stereo enhancement
- Optional stereo headphone output with 32 Ohm drive
  AC '97 2.1 Appendix D re-defines HP_OUT to support True Line Level out functionality
- Optional 18 or 20-bit DAC and ADC resolution
- Optional modem line Codec (ADC and DAC)
  AC '97 2.0 Appendix B fully defines 2-line modem , handset, and GPIO
- Optional 3rd ADC input channel for mic

[1] Down Line Phone

1.2 Audio Codec '97 Architectural Overview

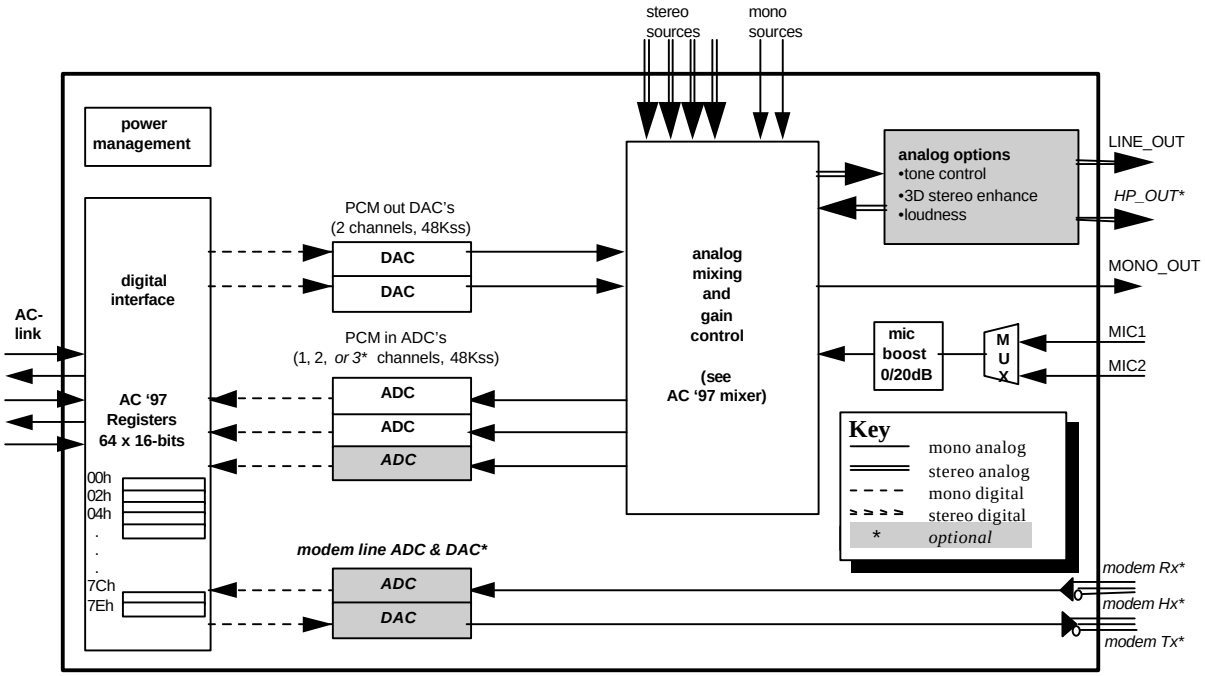


Figure 1. AC '97 1.0 Block Diagram

Figure 1 shows the functional blocks that make up the Audio Codec '97, which is the analog component of a two-chip audio solution (fully described in the next section). The two fixed 48kHz ***or AC '97 2.0 compliant variable rate*** DAC's support a stereo PCM out channel which contains a mix generated in the AC '97 Controller of all software sources, including the internal synthesizer and any other digital sources. PCM out is mixed with additional analog sources, processed with optional 3D stereo enhancement and tone controls, and sent to independently controlled LINE_OUT and HP_OUT, or ***AC '97 2.1 compliant True Line Level Out***. For speakerphone telephony, the MONO_OUT delivers either mic only or a mono mix of sources to the telephony subsystem.

The ADC path supports two channels of fixed 48kHz ***or AC '97 2.0 compliant variable rate*** input, with an option to support a 3rd fixed 48kHz ADC input channel dedicated to the mic. The standard stereo PCM in channel supports record of any mono or stereo source, or a mix of sources[2]. The optional dedicated mic channel extends the range of acoustic echo cancellation capabilities by allowing the audio subsystem to record the MIC along with LINE_OUT (L and R) reference signals needed for robust stereo mic input filtering, either in the AC '97 Controller or on the host CPU. The independent mic channel also has the potential to be dedicated to voice input applications.

The optional ADC and DAC pair supports integration of the line Codec portion of a modem AFE function into AC '97, ***as defined in AC '97 2.0 Appendix B***.

NAMING CONVENTION: Throughout this document signal names have been assigned to be consistent with the point of view of an application running on the PC.

[2] For highest quality and greatest flexibility, the AC '97 controller should provide the capability to *digitally* record any or all of the contributing digital sources in the PCM out mix.

1.3 Integrating AC ‘97 into the System

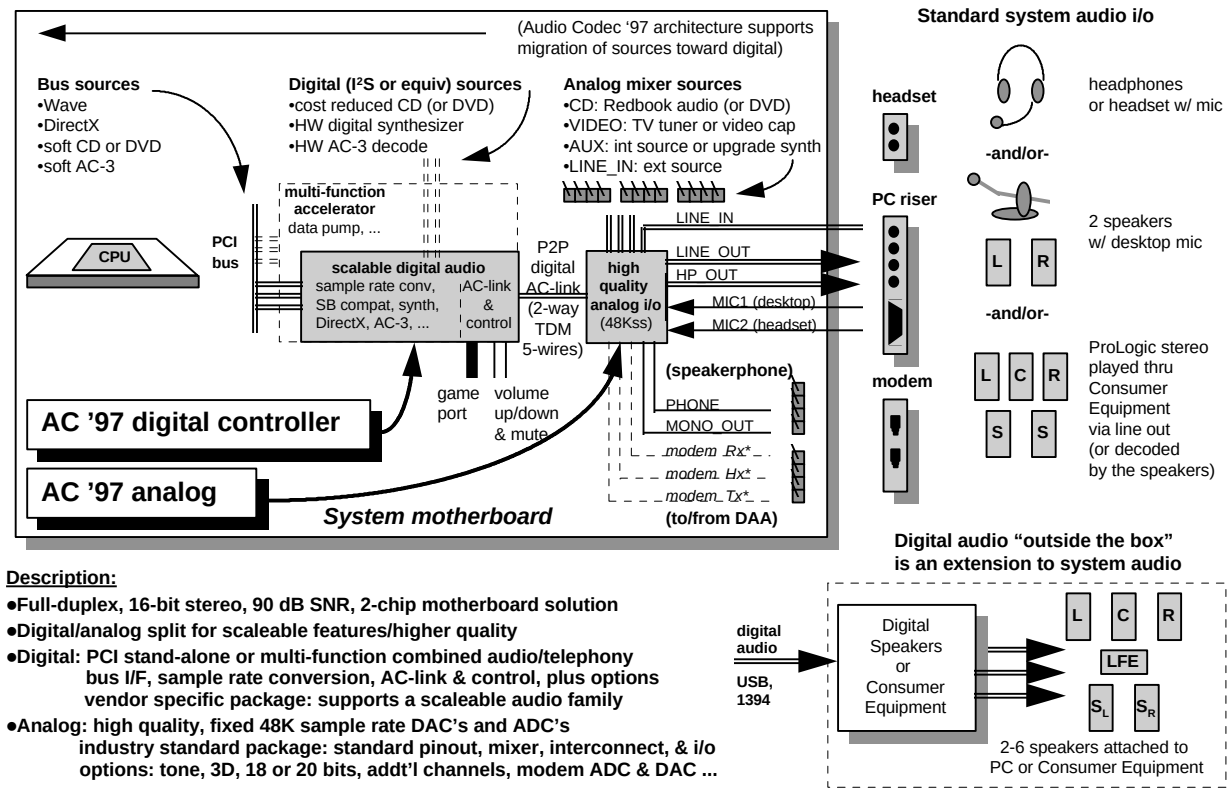


Figure 2. AC ‘97 1.0 System Diagram

The System Diagram in Figure 2 shows the essential features of an AC ‘97 audio design. The AC ‘97 analog component performs fixed 48K ***or AC ’97 2.0 compliant variable*** sample rate DAC & ADC conversions, mixing, and analog processing (tone, 3D stereo enhancement, etc.). It always functions as a slave to an AC ‘97 Digital Controller which must be implemented in the digital portion of any AC ‘97 audio system.

The AC ’97 Controller, primarily targeted for PCI, can be as simple as a stand-alone design which supports high quality sample rate conversions to/from 48kHz, Sound Blaster* compatibility ***(no longer recommended)***, FM ***(no longer recommended)*** and/or wavetable synthesis, with optional DirectSound* acceleration, AC-3 decode, etc. The AC ’97 Controller may also be embedded within a PCI multifunction accelerator, offering higher levels of integration by combining audio with telephony or graphics. However, nothing precludes ISA, USB, or 1394 designs based on the AC ’97 architecture.

The digital link, "AC-link", connecting the AC `97 Controller to the AC `97 analog is a bi-directional, five-wire, serial TDM format interface, designed for dedicated point-to-point interconnect on a circuit board, ***and extended by AC ’97 2.0 Appendix C to support multi-point connections between Controller and up to 4 Codecs.***

The diagram shows the most common (high attach rate) connections, some digital and some analog. PC audio today requires that a number of analog sources be supported in the analog mixer. Over time, it will become attractive from both cost and functionality perspectives to move these sources toward dedicated digital connections or onto the bus[3].

[3] The support for dedicated digital connections requires frequency locking and sample rate conversion capabilities in the AC ’97 controller in order to reconcile independent time bases, the digital source and AC ‘97’s fixed 48kHz.

The AC '97 architecture facilitates this migration. ***AC '97 2.1 Appendix D describes new analog mixer cost reduction options***.

The AC '97 ***1.0*** architecture is designed primarily to support stereo two-speaker PC audio. However, two multi-channel extensions are shown in the system diagram, one utilizing the AC '97 architecture and one independent of it:

- Multi-channel encoded stereo (such as Dolby* ProLogic*) can be played out through the 2-channel AC '97 audio subsystem. This type of signal can be played on normal stereo speakers, decoded into 4-channel by the speakers, or sent to consumer equipment via a stereo analog line out connection.
- True 2/4/6 channel digital audio output (such as 5.1 channel Dolby AC-3*) can bypass the 2-channel AC '97 audio subsystem and be transmitted via a digital link (such as USB or 1394) to digital speakers or digital ready consumer equipment which drives a multi-speaker arrangement such as the home theater[4].

The AC '97 2.0 architecture, specifically Appendix A, defines support for up to 20-bit 6-channel audio at 96 kHz.

1.4 Software Driver support and AC '97 Controller / AC '97 Interoperability

Regardless of the bus and level of integration chosen, the driver written for the AC '97 Controller is responsible for exposing and managing the AC '97 analog features. Interoperability requires that every AC '97 Controller and AC '97 driver ***identify and*** support the basic AC '97 features.

Every AC '97 ***1.0*** Controller, ***and every AC '97 2.1 compliant system (either Controller, Codec, of software driver)*** must be capable of performing high quality (~90 dB SNR) sample rate conversions on a minimum of four simultaneous channels (stereo out + stereo in), between a variety of sample rates and 48kHz:

- 8.0, 11.025, 16.0, 22.05, 32.0, 44.1kHz

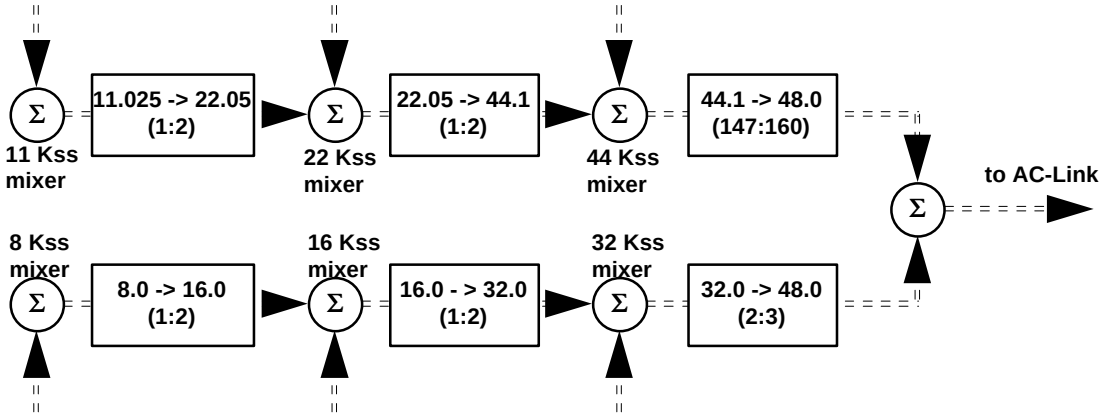
See Appendix D for AC '97 2.1 recommendations and requirements for the digital SRC capability located in the AC '97 2.1 compliant Controller, Codec, or software driver. AC '97 2.1 compliance requires

- ***³85 dB SNR***
- ***³17.64 kHz - 3 dB frequency response***
- ***£-65 dB passband THD+N***
- ***£+/- 0.5 dB passband ripple***

<u>Digital SRC implementation (originally published in the AC '97 Technical FAQ, September 1996):</u>
A PCI based audio system needs to support multiple concurrent input and output sources at diverse sample rates, such as PCM, MIDI, CD digital audio streamed from memory, or decoded AC-3 streamed from memory. The choice is either implement multiple DACs and ADCs running at various sample rates followed by analog mixing, or perform digital sample rate conversion and mixing at one common rate. The digital solution is preferred based on quality, cost and flexibility of implementation.

The following is one possible implementation of digital SRC and mixing which can efficiently support an arbitrary number of digital PCM output sources at any of the standard PC sample rates with a minimum of dedicated SRC hardware resource.

[4] There are many PC audio sources that are still potentially bus independent, such as DOS games, HW accelerated Windows* 95 games, CD Redbook audio, and DVD-ROM subsystems with HW AC-3 decode. In order to hear ALL PC audio sources through one set of digitally connected speakers, backwards compatibility must be addressed.



Annotation Figure: ***Example SRC/mixing implementation***

Mono PCM output always translates in the AC ’97 Controller to two mono channels (L and R) on the AC-link.

The following optional AC ‘97 features should also be supported by all AC ’97 Controller drivers when determined to be present:

- tone control
- loudness
- simulated stereo
- 3D stereo enhancement
- headphone out

Appendix D defines cost reduction options based on elimination of analog mixer features.

Other features may not make sense to support unless there is also support in the AC ‘97 Controller. In these cases interoperability may be limited to an AC ’97 Controller / AC ‘97 analog pair sourced by the same vendor:

- Modem ADC and DAC ***(as defined in AC ’97 2.0 Appendix B)***
- 3rd ADC input channel
- Vendor-specific features

2. Packaging

The 48-pin package has become very popular for 2-channel audio-only Codecs; and vendors of such Codecs are recommended to follow the 48-pin package assignments as closely as possible. The 64-pin package assignments do not match updated recommendations for modem implementations provided in AC '97 2.0 Appendix B, and are now entirely vendor specific.

The AC '97 component is available in two industry standard QFP packages: a 7mm x 7mm body 48-pin package, and a 10mm x 10mm body 64-pin package. Both packages offer SQFP and TQFP versions.

The standard 48-pin package offers OEM's a very attractive motherboard footprint (9x9=81sq mm including pads) but may force the AC '97 vendor to make implementation tradeoffs between optional features, fabrication process, die size capacity, and available pins. The AC '97 Working Group believes that the 48-pin package is attractive for migrating *baseline motherboard audio* to the high quality two-chip PCI audio solution in 1997.

The standard 64-pin package, ***now entirely vendor specific***, offers both OEM's and the AC '97 vendor the potential for higher levels of integration and more optional features, but increases the footprint (12x12=144sq mm including pads). The benefits of the 64-pin package are increased die size capacity, and 16 additional pins which support dedicated features, an additional analog power and ground, and reserved headroom for future expansion. The AC '97 Working Group believes that the 64-pin package is attractive for *highly integrated motherboard* PCI solutions which combine audio with telephony, and ideal for *high performance add-in cards*, as well as *external "digital audio"* solutions on USB or 1394.

2.1 48-pin QFP package

Figure 3 shows the ***original*** pinout for the 48-pin package. Figure 4 shows the package mechanicals. Table 1 gives the ***revised*** pinlist, ***which includes the AC ’97 2.1 Appendix D re-assignments***.

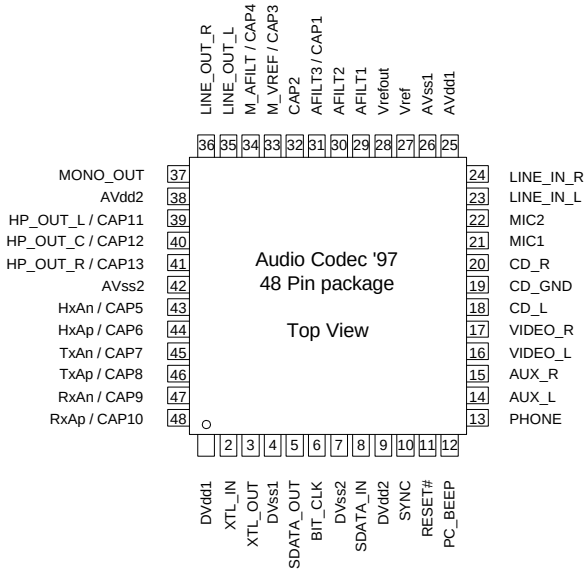
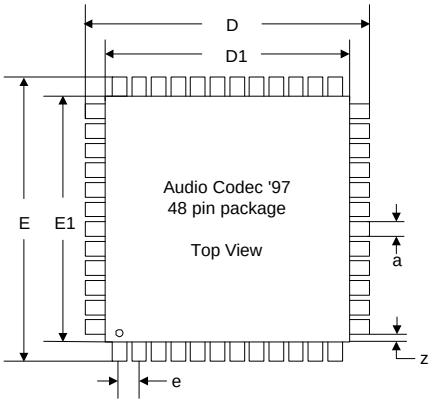


Figure 3. AC ‘97 48-pin package and pinout



Key	Dimension
D	9.00 mm
D1	7.00 mm
E	9.00 mm
E1	7.00 mm
a (lead width)	0.20 mm
e (pitch)	0.50 mm
z	1.00 mm

Figure 4. AC ‘97 48-pin package dimensions

Pin #	Signal Name	Pin#	Signal Name
1	DVdd1	25	AVdd1
2	XTL_IN	26	AVss1
3	XTL_OUT	27	Vref
4	DVss1	28	Vrefout
5	SDATA_OUT	29	AFILT1
6	BIT_CLK	30	AFILT2
7	DVss2	31	AFILT3 / CAP1
8	SDATA_IN	32	CAP2
9	DVdd2	33	M_VREF / CAP3
10	SYNC	34	M_AFILT / CAP4
11	RESET#	35	LINE_OUT_L
12	PC_BEEP	36	LINE_OUT_R
13	PHONE	37	MONO_OUT
14	AUX_L	38	AVdd2
15	AUX_R	39	***LNLVL_OUT_L*** / HP_OUT_L / CAP11
16	VIDEO_L	40	HP_OUT_C / CAP12
17	VIDEO_R	41	***LNLVL_OUT_R*** / HP_OUT_R / CAP13
18	CD_L	42	AVss2
19	CD_GND	43	HxAn / CAP5
20	CD_R	44	HxAp / CAP6
21	MIC1	45	***ID0#*** / TxAn / CAP7
22	MIC2	46	***ID1#*** / TxAp / CAP8
23	LINE_IN_L	47	***EAPD*** / RxAn / CAP9
24	LINE_IN_R	48	***Vendor specific*** / RxAp / CAP10

Table 1. AC '97 48-pin package pinlist

AC '97 2.1 Appendix D discusses external amplified powerdown (EAPD), LINE_OUT, HP_OUT, and consumer equipment (CE) compatible LNLVL_OUT. The pin assignments are as follows:

- ***LNLVL_OUT L,R: pins 39,41***
- ***Codec ID0#,ID1# strapping: pins 45,46***
- ***EAPD pin: pin 47***
- ***Vendor specific: pin 48***

2.2 64-pin QFP package

The original 64-pin package assignments do not match updated AC '97 2.0 recommendations for modem implementations provided in AC '97 2.0 Appendix B, and are now entirely vendor specific.

Figure 5 shows the ***original*** pinout for the 64-pin package. Figure 6 shows the mechanicals. Table 2 gives the ***revised*** pinlist.

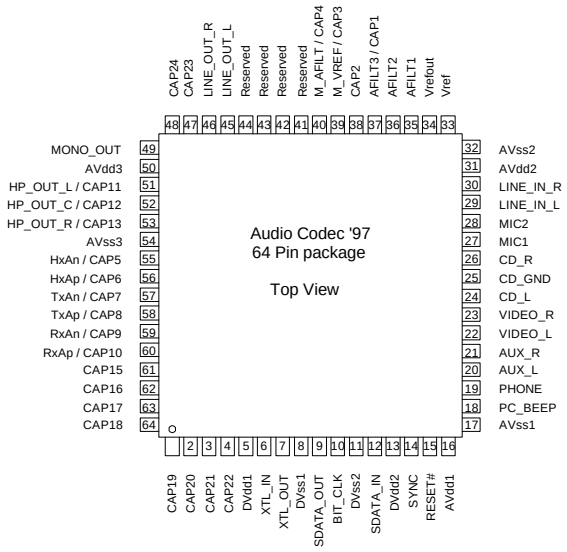
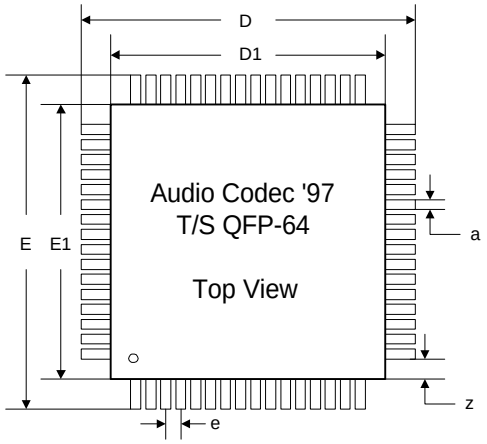


Figure 5. AC '97 64-pin package and pinout



Key	Dimension TQFP
D	12.00 mm
D1	10.00 mm
E	12.00 mm
E1	10.00 mm
a (lead width)	0.20 mm
e (pitch)	0.50 mm
z	1.00 mm

Figure 6. AC '97 64-pin package dimensions

Pin #	Signal Name	Pin#	Signal Name
1	*vendor specific*	33	*vendor specific*
2	*vendor specific*	34	*vendor specific*
3	*vendor specific*	35	*vendor specific*
4	*vendor specific*	36	*vendor specific*
5	*vendor specific*	37	*vendor specific*
6	*vendor specific*	38	*vendor specific*
7	*vendor specific*	39	*vendor specific*
8	*vendor specific*	40	*vendor specific*
9	*vendor specific*	41	*vendor specific*
10	*vendor specific*	42	*vendor specific*
11	*vendor specific*	43	*vendor specific*
12	*vendor specific*	44	*vendor specific*
13	*vendor specific*	45	*vendor specific*
14	*vendor specific*	46	*vendor specific*
15	*vendor specific*	47	*vendor specific*
16	*vendor specific*	48	*vendor specific*
17	*vendor specific*	49	*vendor specific*
18	*vendor specific*	50	*vendor specific*
19	*vendor specific*	51	*vendor specific*
20	*vendor specific*	52	*vendor specific*
21	*vendor specific*	53	*vendor specific*
22	*vendor specific*	54	*vendor specific*
23	*vendor specific*	55	*vendor specific*
24	*vendor specific*	56	*vendor specific*
25	*vendor specific*	57	*vendor specific*
26	*vendor specific*	58	*vendor specific*
27	*vendor specific*	59	*vendor specific*
28	*vendor specific*	60	*vendor specific*
29	*vendor specific*	61	*vendor specific*
30	*vendor specific*	62	*vendor specific*
31	*vendor specific*	63	*vendor specific*
32	*vendor specific*	64	*vendor specific*

Table 2. AC '97 64-pin package pinlist

3. Pin/Signal Descriptions

3.1 Digital I/O

These signals connect the AC ‘97 component to its Controller counterpart and external crystal.

Signal Name	Type	Description
RESET#	I	AC ‘97 Master H/W Reset
XTL_IN	I	24.576 MHz Crystal
XTL_OUT	O	24.576 MHz Crystal
SYNC	I	48 kHz fixed rate sample sync
BIT_ CLK	O ***or I***	12.288 MHz serial data clock ; ***or input for Secondary Codecs***
SDATA_OUT	I	Serial, time division multiplexed, AC ‘97 input stream
SDATA_IN	O	Serial, time division multiplexed, AC ‘97 output stream

Table 3. Digital Signal List

3.2 Analog I/O

These signals connect the AC ‘97 component to analog sources and sinks, including microphones and speakers.

Signal Name	Type	Description
PC_BEEP	I	PC Speaker beep pass through
PHONE	I	From telephony subsystem speakerphone (or DLP - Down Line Phone)
MIC1	I	Desktop Microphone Input
MIC2	I	Second Microphone Input
LINE_IN_L	I	Line In Left Channel
LINE_IN_R	I	Line In Right Channel
CD _L	I	CD Audio Left Channel
CD _GND	I	CD Audio analog ground
CD_ R	I	CD Audio Right Channel
VIDEO_L	I	Video Audio Left Channel
VIDEO_R	I	Video Audio Right Channel
AUX_L	I	Aux Left Channel
AUX_R	I	Aux Right Channel
LINE_OUT_L	O	Line Out Left Channel
LINE_OUT_R	O	Line Out Right Channel
LNLVL_OUT_L / HP_OUT_L / CAP11	O	***True Line Level*** / HP Out Left Channel - optional
HP_OUT_C / CAP12	O	Headphone Out Common - optional
LNLVL_OUT_R / HP_OUT_R / CAP13	O	***True Line Level*** / HP Out Right Channel - optional
MONO_OUT	O	To telephony subsystem speakerphone (or DLP - Down Line Phone)
HxAn / CAP5	O	Either Modem DAA - Hybrid interface or Generic Cap
HxAp / CAP6	O	Either Modem DAA - Hybrid interface or Generic Cap
ID0# / TxAn / CAP7	***I or*** O	***ID strap*** / Modem DAA - Hybrid interface or Generic Cap
ID1# / TxAp / CAP8	***I or*** O	***ID strap*** / Either Modem DAA - Hybrid interface or Generic Cap
EAPD / RxAn / CAP9	***O or*** I	***EAPD*** / Modem DAA - Hybrid interface or Generic Cap
Vendor specific / RxAp / CAP10	***O or*** I	***Vendor specific*** / Modem DAA - Hybrid interface or Generic Cap

Table 4. Analog Signal List

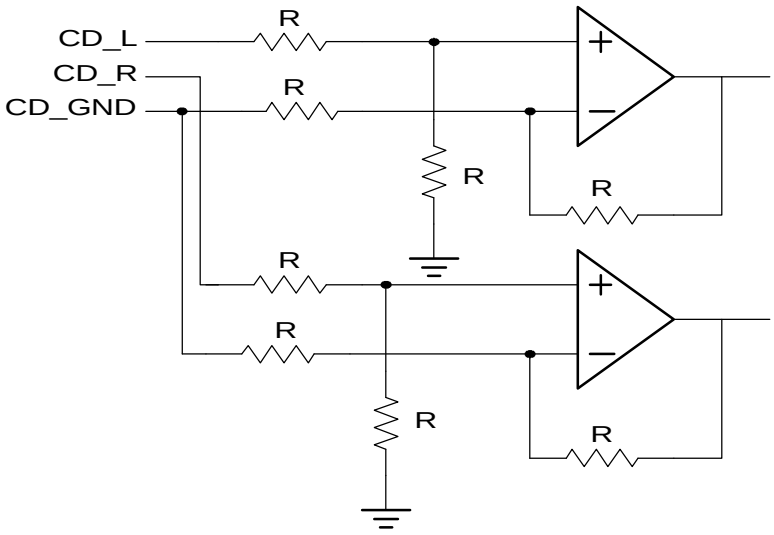


Figure 7. "Conceptual" example of CD circuit inside of AC '97

3.3 Filter/References

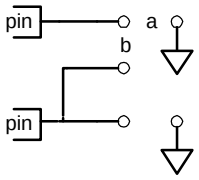
These signals are connected to resistors, capacitors, or specific voltages.

Signal Name	Type	Description
Vref	O	Reference Voltage
Vrefout	O	Reference Voltage out 5mA drive (intended for mic bias)
AFILT1	O	Anti-Aliasing Filter Cap - ADC channel
AFLIT2	O	Anti-Aliasing Filter Cap - ADC channel
AFILT3 / CAP1	O	Anti-Aliasing Filter Cap - optional Mic ADC channel
M_Vref / CAP3	O	Either Modem Reference Voltage or Generic Cap
M_AFILT / CAP4	O	Either Modem Anti-Aliasing Filter Cap or Generic Cap
HxAn / CAP5	O	Either Modem DAA - Hybrid interface or Generic Cap
HxAp / CAP6	O	Either Modem DAA - Hybrid interface or Generic Cap
ID0# / TxAn / CAP7	***I or*** O	***ID0#*** / Modem DAA - Hybrid interface or Generic Cap
ID0# / TxAp / CAP8	***I or*** O	***ID1#*** / Modem DAA - Hybrid interface or Generic Cap
EAPD / RxAn / CAP9	***I or*** O	***EAPD*** / Modem DAA - Hybrid interface or Generic Cap
Vendor specific / RxAp / CAP10	***I or*** O	***Vendor specific*** / Modem DAA - Hybrid interface or Generic Cap
HP_OUT_L / CAP11	O	Headphone out or Generic Cap
HP_OUT_C / CAP12	O	Headphone out or Generic Cap
HP_OUT_R / CAP13	O	Headphone out or Generic Cap
CAP2	O	Generic Cap

Table 5. Filtering and Voltage References

The generic capacitor pins can be used internally to support 3D stereo enhancement, tone control, or other vendor-specific functions. The specific use of each capacitor pin is left up to the AC ‘97 vendor. However, to support a vendor-independent AC ‘97 layout, the following are recommended:

- internal functions which use generic capacitors between pins should always use odd-even (n, n+1) cap pairs, (i.e. 1-2, 3-4, 5-6, 7-8, 9-10, 11-12, etc.)
- internal functions which use generic capacitor to ground may use any cap
- generic capacitor values should be no greater than 1uF (0805 package or smaller is preferred)



To configure capacitor to gnd:
a = capacitor, b = open
To configure capacitor pin to pin:
a = open, b = capacitor

Figure 8. Example of vendor-independent external capacitor layout

3.4 Power and Ground Signals

AC ’97 2.1 Appendix D updates all AC ’97 electrical specifications, including 3.3 V digital operation. This section 3.4 and all of chapter 9 are NOT recommended for new designs.

It is recommended that the digital AC-link interface portion of the AC `97 component be capable of operating at either 5V or 3.3V, depending on which DVdd is supplied. For this reason the digital low and high level voltages are specified as percentages of DVdd (see DC Characteristics in Section 9). The following are clarifications:

- AC ‘97 digital runs at DVdd = 5V, DVdd = 3.3V, or either 5V or 3V (recommended).
- All DVdd inputs are the same level, 5V or 3.3V.
- When designed in the system AC '97 Controller / AC '97 pairs always run off the same DVdd level.
- AC '97 analog runs at AVdd = 5V or AVdd = 3.3V.
- All AVdd inputs are the same level, 5V or 3.3V.
- DVdd and AVdd can be different levels.

Signal Name	Type	Description
AVdd1	I	Analog Vdd - 5.0V or 3.3V
AVdd2	I	Analog Vdd - 5.0V or 3.3V
AVss1	I	Analog Gnd
AVss2	I	Analog Gnd
DVdd1	I	Digital Vdd - 5.0V, 3.3V, or either 5V or 3.3V
DVdd2	I	Digital Vdd - 5.0V, 3.3V, or either 5V or 3.3V
Dvss1	I	Digital Gnd
Dvss2	I	Digital Gnd

Table 6. Power Signal List

4. System Usage

4.1 AC ‘97 Connection to the Digital AC ’97 Controller

AC ‘97 communicates with its companion AC ‘97 Controller via a digital serial link, AC-link. All digital audio streams, optional modem line Codec streams, and command/status information are communicated over this point-to-point serial interconnect. A breakout of the signals connecting the two is shown in Figure 9. For a detailed description of the AC-link, refer to Section 5.

For a detailed description of ***AC ’97 2.1 compliant multi-point operation see Appendices C and D.***

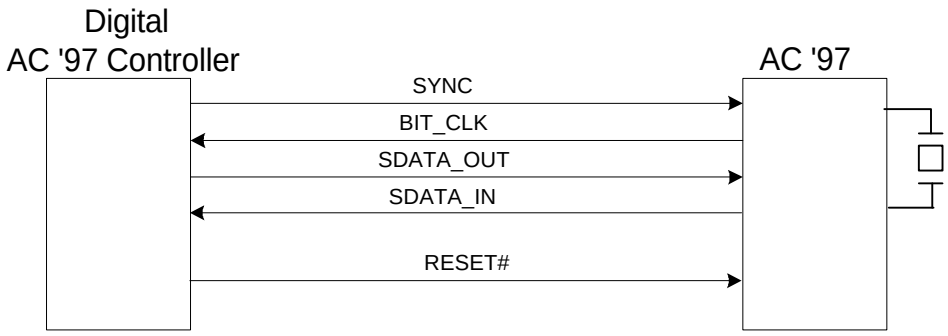


Figure 9. AC ‘97 connection to its companion AC ‘97 Controller

4.2 Clocking

AC '97 derives its clock internally from an externally attached 24.576 MHz crystal[5], and drives a buffered and divided down (1/2) clock to its digital companion Controller over AC-link under the signal name "BIT_CLK". Clock jitter at the DACs and ADCs is a fundamental impediment to high quality output, and the internally generated clock will provide AC '97 with a clean clock that is independent of the physical proximity of AC '97's companion Digital Controller (henceforth referred to as the "AC '97 Controller").

The beginning of all audio sample packets, or Audio Frames, transferred over AC-link is synchronized to the rising edge of the SYNC signal. SYNC is driven by the AC '97 Controller. The AC '97 Controller takes BIT_CLK as an input and generates SYNC by dividing BIT_CLK by 256 and applying some conditioning to tailor its duty cycle. This yields a 48kHz SYNC signal whose period defines an audio frame. Data is transitioned on AC-link on every rising edge of BIT_CLK, and subsequently sampled on the receiving side of AC-link on each immediately following falling edge of BIT_CLK.

4.3 Resetting AC '97

There are three types of AC '97 reset:

1. a *cold* reset where all AC '97 logic (registers included) is initialized to its default state
2. a *warm* reset where the contents of the AC '97 register set are left unaltered
3. a *register* reset which only initializes the AC '97 registers to their default states

After signaling a reset to AC '97, the AC '97 Controller should not attempt to play or capture audio data until it has sampled a "Codec Ready" indication from AC '97. Refer to section 5 for details.

[5] The use of crystal is recommended, but an external oscillator may also be input to AC '97 XTAL_IN

5. Digital Interface

5.1 AC-link Digital Serial Interface Protocol

AC ‘97 incorporates a 5 pin digital serial interface that links it to the AC ’97 Controller. AC-link is a bi-directional, fixed rate, serial PCM digital stream. It handles multiple input, and output audio streams, as well as control register accesses employing a time division multiplexed (TDM) scheme. The AC-link architecture divides each audio frame into 12 outgoing and 12 incoming data streams, each with 20-bit sample resolution. With a minimum required DAC and ADC resolution of 16-bits, AC ‘97 could also be implemented with 18 or 20-bit DAC/ADC resolution, given the headroom that the AC-link architecture provides.

The control and data slots defined by AC ‘97 1.0 include:

- **SDATA_OUT TAG** **1 output slot** **(0)**
- **SDATA_IN TAG** **1 input slot** **(0)**
- **Control (CMD ADDR & DATA) write port** **2 output slots** **(1,2)**
- **Status (STATUS ADDR & DATA) read port** **2 input slots** **(1,2)**
- **PCM L & R DAC Playback** **2 output slots** **(3,4)**
- **PCM L & R ADC Record** **2 input slots** **(3,4)**
- **Optional Modem Line 1 DAC** **1 output slot** **(5)**
- **Optional Modem Line 1 ADC** **1 input slot** **(5)**
- **Optional Dedicated Microphone ADC** **1 input slot** **(6)**

The control and data slots defined by AC ‘97 2.0 include:

- ***Optional 6-channel PCM playback*** ***4 output slots*** ***(6,7,8,9)***
- ***Optional Modem Line 2, handset output*** ***2 output slots*** ***(10,11)***
- ***Optional Modem Line 2, handset input*** ***2 input slots*** ***(10,11)***
- ***Optional Modem IO control*** ***1 output slot*** ***(12)***
- ***Optional Modem IO status*** ***1 input slot*** ***(12)***

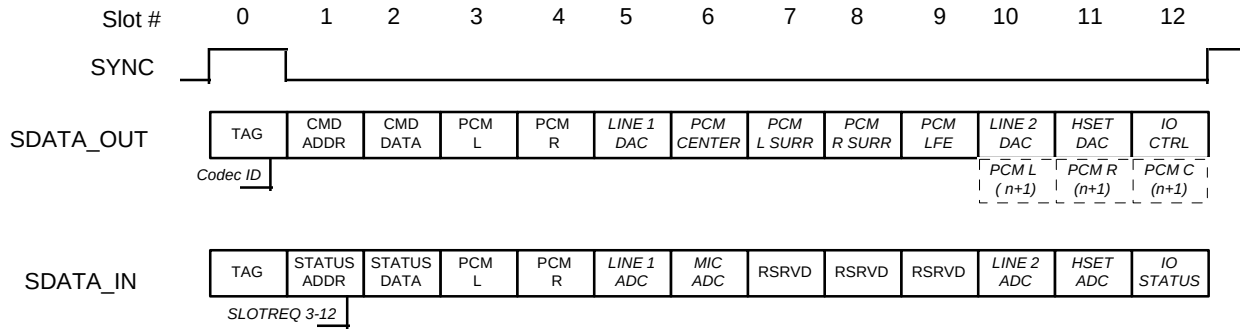


Figure 10. AC ‘97 Standard Bi-directional Audio Frame

The AC ‘97 Controller signals synchronization of all AC-link data transactions. AC ‘97 drives the serial bit clock onto AC-link, which the AC ’97 Controller then qualifies with a synchronization signal to construct audio frames.

SYNC, fixed at 48 kHz, is derived by dividing down the serial bit clock (BIT_CLK). BIT_CLK, fixed at 12.288 MHz, provides the necessary clocking granularity to support 12, 20-bit outgoing and incoming time slots. AC-link serial data is transitioned on each rising edge of BIT_CLK. The receiver of AC-link data, AC ‘97 for outgoing data and AC ’97 Controller for incoming data, samples each serial bit on the falling edges of BIT_CLK.

The AC-link protocol provides for a special 16-bit[6] time slot (Slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A 1 in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream, and contains valid data. If a slot is tagged invalid, it is the responsibility of the source of the data, (AC ‘97 for the input stream, AC ’97 Controller for the output stream), to stuff all bit positions with 0’s during that slot’s active time.

SYNC remains high for a total duration of 16 BIT_CLKs at the beginning of each audio frame. The portion of the audio frame where SYNC is high is defined as the Tag Phase. The remainder of the audio frame where SYNC is low is defined as the “Data Phase”.

Additionally, for power savings, all clock, sync, and data signals can be halted. This requires that AC ‘97 be implemented as a static design to allow its register contents to remain intact when entering a power savings mode.

5.1.1 AC-link Audio Output Frame (SDATA_OUT)

The audio output frame data streams correspond to the multiplexed bundles of all digital output data targeting AC ‘97’s DAC inputs, and control registers. As briefly mentioned earlier, each audio output frame supports up to 12 20-bit outgoing data time slots. Slot 0 is a special reserved time slot containing 16-bits which are used for AC-link protocol infrastructure.

5.1.1.1 Slot 0: TAG

Within slot 0 the first bit is a global bit (SDATA_OUT slot 0, bit 15) which flags the validity for the entire audio frame. If the “Valid Frame” bit is a 1, this indicates that the current audio frame contains at least one slot time of valid data. The next 12 bit positions sampled by AC ‘97 indicate which of the corresponding 12 time slots contain valid data. In this way data streams of differing sample rates can be transmitted across AC-link at its fixed 48 kHz audio frame rate[7].

Figure 11 illustrates the time slot based AC-link protocol. ***(Please note that Bits 1 and 0 of slot 0 tag phase are now used for AC ’97 2.x compliant multi-point Codec addressing as described in AC ’97 2.0 Appendix C).***

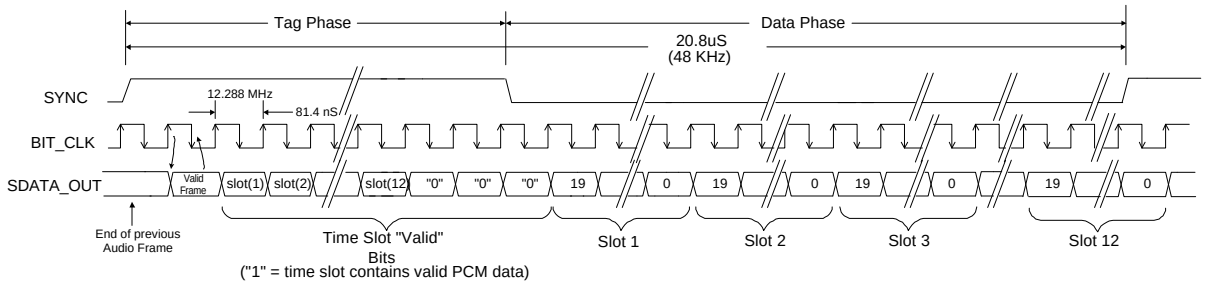


Figure 11. AC-link Audio Output Frame

A new audio output frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, AC ‘97 samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the AC ’97 Controller transitions SDATA_OUT into the first bit position of slot 0 (Valid Frame bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled by AC ‘97 on the following falling edge of BIT_CLK. This sequence ensures that data transitions, and subsequent sample points for both incoming and outgoing data streams are time aligned.

[6] 15-bits defined, with 1 reserved.

[7] Control/Status as well as optional extensions of the baseline AC ‘97 specification, such as the modem line Codec, may take advantage of this feature. ***See AC ’97 2.x Appendices A-D for full description of the standardized variable rate signaling protocols.***

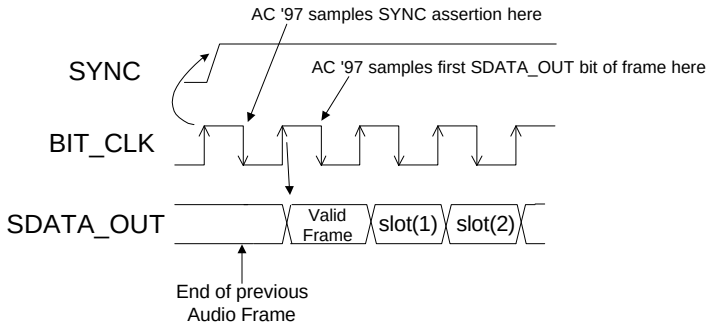


Figure 12. Start of an Audio Output Frame

SDATA_OUT’s composite stream is MSB justified (MSB first) with all non-valid slots’ bit positions stuffed with 0’s by the AC ’97 Controller.

If there are less than 20 valid bits within an assigned and valid time slot, the AC ’97 Controller always stuffs all trailing non-valid bit positions of the 20-bit slot with 0’s.

As an example, consider an 8-bit sample stream that is being played out to one of AC ‘97’s DACs. The first 8-bit positions are presented to the DAC (MSB justified) followed by the next 12 bit-positions which are stuffed with 0’s by the AC ’97 Controller. This ensures that regardless of the resolution of the implemented DAC (16, 18 or 20-bit), no DC biasing will be introduced by the least significant bits.

When mono audio sample streams are output from the AC ’97 Controller it is necessary that BOTH left and right sample stream time slots be filled with the same data.

5.1.1.2 Slot 1: Command Address Port

The command port is used to control features, and monitor status (see Audio Input Frame Slots 1 and 2) for AC ‘97 functions including, but not limited to, mixer settings, and power management (refer to the control register section of this specification).

The control interface architecture supports up to 64 16-bit read/write registers, addressable on even byte boundaries, ***and reserves support for 64 odd addresses, as described in AC ’97 2.1 Appendix D***. Only the even registers (00h, 02h, etc.) are currently defined, odd register (01h, 03h, etc.) accesses are reserved.

Note that shadowing of the control register file on the AC ’97 Controller is an option left open to the implementation of the AC ’97 Controller. AC ‘97’s control register file is nonetheless required to be readable as well as writeable to provide more robust testability.

Audio output frame slot 1 communicates control register address, and write/read command information to AC ‘97.

Command Address Port bit assignments:

Bit(19)	Read/Write command	(1=read, 0=write)
Bit(18:12)	Control Register Index	(64 16-bit locations, addressed on even byte boundaries)
Bit(11:0)	Reserved	(Stuffed with 0’s)

The first bit (MSB) sampled by AC ‘97 indicates whether the current control transaction is a read or a write operation. The following 7 bit positions communicate the targeted control register address. The trailing 12 bit positions within the slot are reserved and must be stuffed with 0’s by the AC ’97 Controller.

5.1.1.3 Slot 2: Command Data Port

The command data port is used to deliver 16-bit control register write data in the event that the current command port operation is a write cycle. (as indicated by Slot 1, bit 19)

Bit(19:4)	Control Register Write Data	(Stuffed with 0’s if current operation is a read)
Bit(3:0)	Reserved	(Stuffed with 0’s)

If the current command port operation is a read then the entire slot time must be stuffed with 0’s by the AC ’97 Controller.

5.1.1.4 Slot 3: PCM Playback Left Channel

Audio output frame slot 3 is the composite digital audio left playback stream. In a typical ‘Games Compatible” PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC ’97 Controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is transferred, the AC ’97 Controller must stuff all trailing non-valid bit positions within this time slot with 0’s.

5.1.1.5 Slot 4: PCM Playback Right Channel

Audio output frame slot 4 is the composite digital audio right playback stream. In a typical ‘Games Compatible” PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC ’97 Controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is transferred, the AC ’97 Controller must stuff all trailing non-valid bit positions within this time slot with 0’s.

5.1.1.6 Slot 5: Optional Modem Line 1 DAC

Audio output frame slot 5 contains the MSB justified modem DAC input data (if the line Codec is supported).

The optional modem DAC resolution is by default 16-bits. During normal runtime operation the AC ’97 Controller is then responsible for stuffing any non-valid trailing bit positions within this time slot with 0’s.

See AC ’97 2.0 Appendix B for full details on modem implementation.

5.1.1.7 Slots 6-9: Optional PCM Center, L Surround, R Surround, and LFE DACs

See AC ’97 2.0 Appendix A.

5.1.1.8 Slot 10: Optional Modem Line 2 DAC

See AC ’97 2.0 Appendix B.

5.1.1.9 Slot 11: Optional Modem Headset DAC

See AC ’97 2.0 Appendix B.

5.1.1.10 Slot 12: Optional Modem GPIO control

See AC ’97 2.0 Appendix B.

5.1.2 AC-link Audio Input Frame (SDATA_IN)

The audio input frame data streams correspond to the multiplexed bundles of all digital input data targeting the AC ’97 Controller. As is the case for audio output frame, each AC-link audio input frame consists of 12, 20-bit time slots. Slot 0 is a special reserved time slot containing 16-bits which are used for AC-link protocol infrastructure.

5.1.2.1 Slot 0: TAG

Within slot 0 the first bit is a global bit (SDATA_IN slot 0, bit 15) which flags whether AC ‘97 is in the “Codec Ready” state or not. If the “Codec Ready” bit is a 0, this indicates that AC ‘97 is not ready for normal operation. This condition is normal following the deassertion of power on reset for example, while AC ‘97’s voltage references settle. When the AC-link “Codec Ready” indicator bit is a 1 it indicates that the AC-link and AC ‘97 control and status registers are in a fully operational state. The AC ‘97 Controller must further probe the Powerdown Control/Status Register (section 6.3) to determine exactly which subsections, if any, are ready.

Prior to any attempts at putting AC ‘97 into operation the AC ’97 Controller should poll the first bit in the audio input frame (SDATA_IN slot 0, bit 15) for an indication that AC ‘97 has gone “Codec Ready”. Once AC ‘97 is sampled “Codec Ready”[8] then the next 12 bit positions sampled by the AC ’97 Controller indicate which of the

[8] There are several subsections within AC ‘97 that can independently go busy/ready. It is the responsibility of the

corresponding 12 time slots are assigned to input data streams, and that they contain valid data. The following diagram illustrates the time slot-based AC-link protocol.

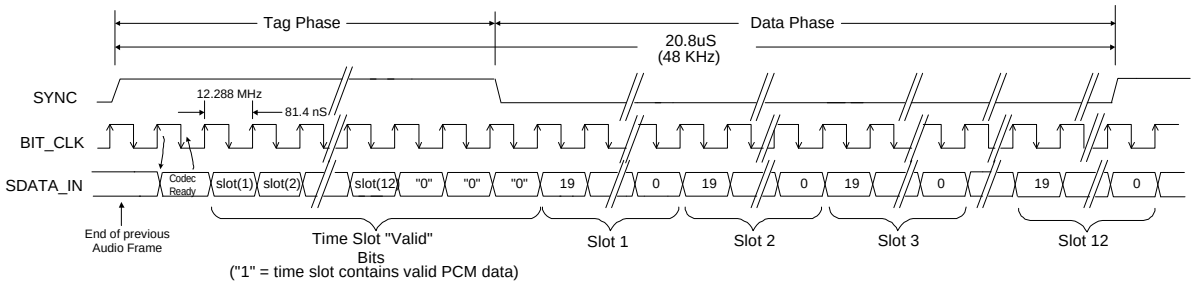


Figure 13. AC-link Audio Input Frame

A new audio input frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, AC ‘97 samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising of BIT_CLK, AC ‘97 transitions SDATA_IN into the first bit position of slot 0 (“Codec Ready” bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled by the AC ’97 Controller on the following falling edge of BIT_CLK. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing data streams are time aligned.

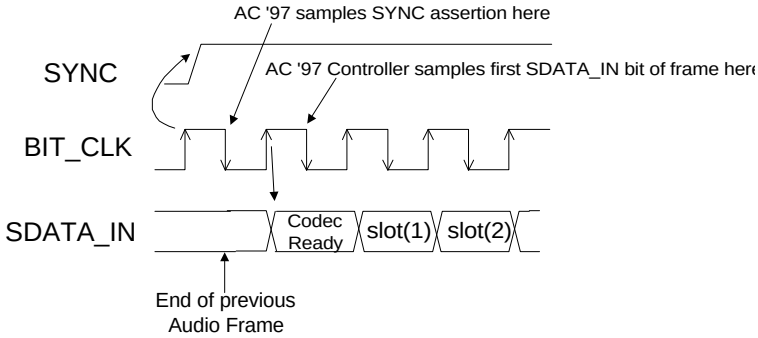


Figure 14. Start of an Audio Input Frame

SDATA_IN’s composite stream is MSB justified (MSB first) with all non-valid bit positions (for assigned and/or unassigned time slots) stuffed with 0’s by AC ‘97. SDATA_IN data is sampled on the falling edges of BIT_CLK .

5.1.2.2 Slot 1: Status Address Port

The status port is used to monitor status for AC ‘97 functions including, but not limited to, mixer settings and power management (refer to section 6.3 of this specification).

Audio input frame slot 1’s stream echoes the control register index, for historical reference, for the data to be returned in slot 2. (Assuming that slots 1 and 2 had been tagged “valid” by AC ‘97 during slot 0.)

AC ’97 controller to probe more deeply into the AC ‘97 register file to determine which AC ‘97 subsections are actually ready (refer to section 6.3 for more information).

Status Address Port bit assignments:

Bit(19)	RESERVED	(Stuffed with 0)
Bit(18:12)	Control Register Index	(Echo of register index for which data is being returned)
Bit(11:2)	***SLOTREQ bits***	***See AC ’97 2.0 Appendix A SLOTREQ bit definitions***
Bit(1,0)	RESERVED	(Stuffed with 0’s)

The first bit (MSB) generated by AC ‘97 is always stuffed with a 0. The following 7 bit positions communicate the associated control register address, ***the next 10 bits support the AC ’97 2.0 variable sample rate signaling protocol as described in Appendix A***, and the trailing 2 bit positions are stuffed with 0’s by AC ‘97.

5.1.2.3 Slot 2: Status Data Port

The status data port delivers 16-bit control register read data.

Bit(19:4)	Control Register Read Data	(Stuffed with 0’s if tagged “invalid” by AC ‘97)
Bit(3:0)	RESERVED	(Stuffed with 0’s)

If Slot 2 is tagged invalid by AC ‘97, then the entire slot will be stuffed with 0’s by AC ‘97.

5.1.2.4 Slot 3: PCM Record Left Channel

Audio input frame slot 3 is the left channel output of AC ‘97’s input MUX, post-ADC.

AC ‘97’s ADCs can be implemented to support 16, 18, or 20-bit resolution.

AC ‘97 ships out its ADC output data (MSB first), and stuffs any trailing non-valid bit positions with 0’s to fill out its 20-bit time slot.

5.1.2.5 Slot 4: PCM Record Right Channel

Audio input frame slot 4 is the right channel output of AC ‘97’s input MUX, post-ADC.

AC ‘97’s ADCs can be implemented to support 16, 18, or 20-bit resolution.

AC ‘97 ships out its ADC output data (MSB first), and stuffs any trailing non-valid bit positions with 0’s to fill out its 20-bit time slot.

5.1.2.6 Slot 5: Optional Modem Line 1 ADC

Audio input frame slot 5 contains MSB justified, modem ADC output data (if the line Codec is supported).

The optional modem ADC resolution is by default 16-bits. All trailing, non-valid bit positions will be stuffed with 0’s to fill out its 20-bit time slot. AC ’97 Controller is then responsible for stuffing any non-valid trailing bit positions within this time slot with 0’s.

See AC ’97 2.0 Appendix B for full details on modem implementation.

5.1.2.7 Slot 6: Optional Dedicated Microphone Record Data

Audio input frame slot 6 is an optional (post-ADC) third PCM system input channel available for dedicated use by a desktop microphone. This input channel would supplement a true stereo output which would then enable a more precise echo cancellation algorithm for speakerphone applications.

AC ‘97’s ADCs can be implemented to support 16, 18, or 20-bit output resolution. Resolution of all PCM input ADC’s, including this optional Mic ADC is reported by the Reset register. If supported AC ‘97 will ship out ADC data of the implemented resolution (MSB first), and stuff any trailing non-valid bit positions with 0’s.

AC ‘97 Controller/AC ’97 pair interoperability can only be guaranteed for non-optional AC ‘97 audio features. An audio component vendor who develops an AC ’97 with optional Dedicated Mic channel support should also offer an AC ’97 Controller to fully support this feature with a matched set solution.

5.1.2.8 Slots 7-9: Reserved

Audio input frame slots 7-9 are reserved for future use and are always stuffed with 0’s by AC ‘97.

5.1.2.9 Slot 10: Optional Modem Line 2 ADC

See AC ’97 2.0 Appendix B.

5.1.2.10 Slot 11: Optional Modem Headset ADC

See AC ’97 2.0 Appendix B.

5.1.2.11 Slot 12: Optional Modem GPIO status

See AC ’97 2.0 Appendix B.

5.2 AC-link Low Power Mode

The AC-link signals can be placed in a low power mode (see section 6.3). When AC ‘97’s Powerdown Register (26h), is programmed to the appropriate value, both BIT_CLK and SDATA_IN will be brought to and held at a logic low voltage level.

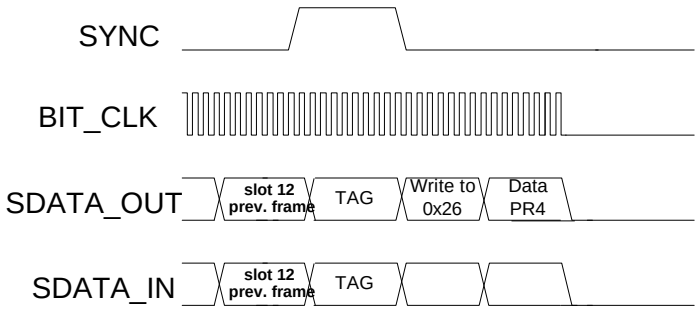


Figure 15. AC-link Powerdown Timing

BIT_CLK and SDATA_IN are transitioned low immediately[9] following the decode of the write to the Powerdown Register (26h) with PR4. When the AC ’97 Controller driver is at the point where it is ready to program the AC-link into its low power mode, slots (1 and 2) ARE ASSUMED TO BE the only valid stream in the audio output frame[10].

The AC ’97 Controller should also drive SYNC, and SDATA_OUT low after programming AC ‘97 to this low power, halted mode. ***The AC ’97 Controller is required to drive, and keep SYNC and SDATA_OUT low in this low power, halted mode.***

See AC ’97 2.1 Appendix D for additional discussion of power management.

Once AC ‘97 has been instructed to halt BIT_CLK, a special “wake-up” protocol must be used to bring the AC-link to the active mode since normal audio output and input frames can not be communicated in the absence of BIT_CLK.

5.2.1 Waking up the AC-link

There are two methods for bringing the AC-link out of a low power, halted mode. Regardless of the method, it is the AC ’97 Controller that performs the wake-up task.

AC-link protocol provides for a “Cold AC ‘97 Reset”, and a “Warm AC ‘97 Reset”. The current power down state would ultimately dictate which form of AC ‘97 reset is appropriate. Unless a “cold” or “register” reset (a write to the Reset register) is performed, wherein the AC ‘97 registers are initialized to their default values, registers are required to keep state during all power down modes.

Once powered down, re-activation of the AC-link via re-assertion of the SYNC signal must not occur for a

[9] Within the maximum specified time.
[10] At this point in time it is assumed that all sources of audio input have also been neutralized.

minimum of four audio frame times following the frame in which the power down was triggered. When AC-link powers up it indicates readiness via the Codec Ready bit (input slot 0, bit 15).

See AC ’97 2.1 Appendix D for additional discussion of power management.

5.2.1.1 Cold AC ‘97 Reset

A cold reset is achieved by asserting RESET# for the minimum specified time. By driving RESET# low, BIT_CLK, and SDATA_OUT will be activated, or re-activated as the case may be, and all AC ‘97 control registers will be initialized to their default power on reset values.

RESET# is an asynchronous AC ‘97 input.

See AC ’97 2.1 Appendix D for additional discussion of power management.

5.2.1.2 Warm AC ‘97 Reset

A warm AC ‘97 reset will re-activate the AC-link without altering the current AC ‘97 register values. A warm reset is signaled by driving SYNC high for a minimum of 1us in the absence of BIT_CLK.

Within normal audio frames SYNC is a synchronous AC ‘97 input. However, in the absence of BIT_CLK, SYNC is treated as an asynchronous input used in the generation of a warm reset to AC ‘97.

AC ‘97 MUST NOT respond with the activation of BIT_CLK until SYNC has been sampled low again by AC ‘97. This will preclude the false detection of a new audio frame.

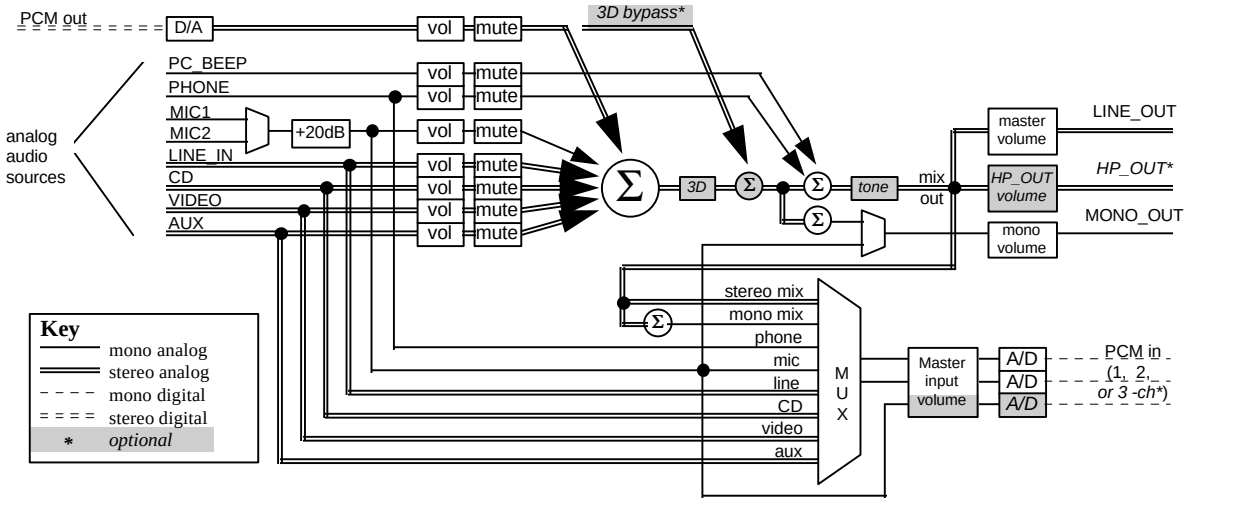
See AC ’97 2.1 Appendix D for additional discussion of power management.

6. AC ‘97 Mixer

The AC ‘97 mixer is designed to manage playback and record of all digital and analog audio sources likely to be present in the 1997 high volume PC. These include:

- **System audio**: digital PCM input and output for business, games, and multimedia
- **CD/DVD:** analog CD/DVD-ROM Redbook audio with internal connections to Codec mixer
- **Mono microphone**: choice of desktop or headset mic, with programmable boost and gain
- **Speakerphone**: use of system mic & speakers for telephony, DSVD, and video conferencing
- **Stereo line in**: analog external line level source from consumer audio, video camera, etc
- **Video:** TV tuner or video capture card with internal connections to Codec mixer
- **AUX/synth**: analog FM or wavetable synthesizer, or other internal source

AC ’97 2.1 Appendix D defines cost reduction options based on elimination of certain analog mixer features.



source	function	connection
PC_BEEP	PC beep pass thru	from PC beeper output
PHONE	speakerphone or DLP in	from telephony subsystem
MIC1	desktop microphone	from mic jack
MIC2	headset microphone	from headset mic jack
LINE_IN	external audio source	from line in jack
CD	audio from CD-ROM drive	cable from CD-ROM
VIDEO	audio from TV tuner or video camera	cable from TV or VidCap card
AUX	upgrade synth or other external source	internal connector
PCM out	digital audio output from AC '97 Controller	AC-link
mix out	mix of all sources	AC ‘97 internal
LINE_OUT	stereo mix of all sources	to output jack
HP_OUT	stereo mix of all sources	to headphone jack
MONO_OUT	mic or mix for speakerphone or DLP out	to telephony subsystem
PCM in	digital audio input to AC '97 Controller	AC-link

Output MIX supports:
- stereo mix of all sources for LINE_OUT
- mono mic or mix for MONO_OUT
- *optional HP_OUT for headphone**
- *optional 3D and tone control**
- *PCM out can be mixed pre or post 3D**

Input MUX supports:
- select from 1, 2, *or 3** channels
- any mono or stereo source
- mono or stereo mix of all sources
- 2-ch input w/ output ref (mic + mono mix)
- *3rd channel dedicated to mic**
- *3-ch input w/ output ref (mic + stereo mix)**

Figure 16. AC ‘97 Mixer Functional Diagram

6.1 Mixer output

The AC ‘97 mixer generates two distinct outputs:

- a stereo mix of all sources for output to the speakers, headset, and line out (LINE_OUT and HP_OUT)
- a mono, mic only or mix of all sources (minus PHONE and PC_BEEP) for speakerphone out (MONO_OUT)

6.1.1 PCM out path and optional 3D bypass

If analog 3D stereo enhancement is supported in AC ‘97 it is desirable that the PCM out source be mixable pre- or post-analog 3D processing. This allows digital 3D audio (rendered with volume, pan, reverb, Doppler, HRTF, etc.) on PCM out to bypass the analog 3D processing regardless of whether analog 3D is enabled or disabled. This prevents “smearing” of digital 3D audio, and also enables digital 3D audio sources to be mixed with 3D stereo enhanced analog sources (CD, AUX, etc).

The default PCM out path is through volume, mute, and analog 3D stereo enhancement. However, if the AC ’97 Controller implements digital 3D audio, and detects analog 3D stereo enhancement support in the AC ’97 analog, it can enable the 3D bypass path. This capability to switch to post 3D can also be exposed via API’s to support SW which emulates or accelerates digital 3D rendering.

In either PCM out scenario it is advantageous for the AC ‘97 Controller to use the post D/A analog volume control to support full resolution D/A conversions followed by analog attenuation as a means of achieving high SNR.

6.2 Mixer input

The mixer input is a MUX design which offers the capability to record any of the audio sources or the outgoing mix of all sources. This design is more efficient to implement than an independent input mix, allows the user to apply 3D and tone controls to recordings, and offers simple monitoring when a mix is recorded: what you hear is what you get (WYHIWYG). Mono and stereo mix also provide excellent echo cancellation reference signals.

AC ‘97 supports the full range of input options[11]:

- any mono or stereo source
- mono or stereo mix of all sources
- 2-channel input with mono output reference (mic + mono mix for mono echo cancellation)
- optional 3-channel input with stereo output reference (mic + stereo mix for stereo echo cancellation)

[11] The audio driver should maintain a persistent record input level for each MUX input option.

6.3 Mixer Registers

Table 7 shows the mixer register indexes and usage. All registers not shown and bits containing an X are assumed to be reserved.

AC '97 2.x Appendices A-D expand the register definitions. Appendix D now requires that reserved or non-implemented bits marked X return 0 upon read back.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	na
02h	Master Volume	Mute	X	*ML5*	ML4	ML3	ML2	ML1	ML0	X	X	*MR5*	MR4	MR3	MR2	MR1	MR0	8000h
04h	*Headphone Volume*	*Mute*	*X*	*ML5*	*ML4*	*ML3*	*ML2*	*ML1*	*ML0*	*X*	*X*	*MR5*	*MR4*	*MR3*	*MR2*	*MR1*	*MR0*	*8000h*
06h	*Master Volume Mono*	*Mute*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*MM5*	*MM4*	*MM3*	*MM2*	*MM1*	*MM0*	*8000h*
08h	*Master tone (R & L)*	*X*	*X*	*X*	*X*	*BA3*	*BA2*	*BA1*	*BA0*	*X*	*X*	*X*	*X*	*TR3*	*TR2*	*TR1*	*TR0*	*0F0Fh*
0Ah	*PC_BEEP Volume*	*Mute*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*PV3*	*PV2*	*PV1*	*PV0*	*X*	*x000h*
0Ch	*Phone Volume*	*Mute*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*GN4*	*GN3*	*GN2*	*GN1*	*GN0*	*8008h*
0Eh	Mic Volume	Mute	X	X	X	X	X	X	X	X	20 dB	*X*	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line In Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
14h	*Video Volume*	*Mute*	*X*	*X*	*GL4*	*GL3*	*GL2*	*GL1*	*GL0*	*X*	*X*	*X*	*GR4*	*GR3*	*GR2*	*GR1*	*GR0*	*8808h*
16h	*Aux Volume*	*Mute*	*X*	*X*	*GL4*	*GL3*	*GL2*	*GL1*	*GL0*	*X*	*X*	*X*	*GR4*	*GR3*	*GR2*	*GR1*	*GR0*	*8808h*
18h	PCM Out Vol	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Record Select	X	X	X	X	X	SL2	SL1	SL0	X	X	X	X	X	SR2	SR1	SR0	0000h
1Ch	Record Gain	Mute	X	X	X	GL3	GL2	GL1	GL0	X	X	X	X	GR3	GR2	GR1	GR0	8000h
1Eh	*Record Gain Mic*	*Mute*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*GM3*	*GM2*	*GM1*	*GM0*	*8000h*
20h	*General Purpose*	*POP*	*ST*	*3D*	*LD*	*X*	*X*	*MIX*	*MS*	*LPBK*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*0000h*
22h	*3D Control*	*X*	*X*	*X*	*X*	*CR3*	*CR2*	*CR1*	*CR0*	*X*	*X*	*X*	*X*	*DP3*	*DP2*	*DP1*	*DP0*	*0000h*
24h	*Reserved*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*
26h	Powerdown Ctrl/Stat	EAPD	*PR6*	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	na
28h-3Ah	*AC '97 2.0 Audio See Appendix A*	*A*	*A*	*A*	*A*	*A*	*A*	*A*	*A*	*A*	*A*	*A*	*A*	*A*	*A*	*A*	*A*	*A*
3Ch-58h	*AC '97 2.0 Modem See Appendix B*	*B*	*B*	*B*	*B*	*B*	*B*	*B*	*B*	*B*	*B*	*B*	*B*	*B*	*B*	*B*	*B*	*B*
5Ah-7Ah	*Vendor Reserved*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	na
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	na

Table 7. Mixer Registers

NOTES:

1. *ITALIC UNDERLINE* indicates optional feature registers or optional bits within a register. Whether implemented or not, these may be written to, but reads ~~will be don't care~~ ***must return 0*** if there is no support for the feature.
2. Any reserved bits, marked X, can be written to but ~~are don't care~~ ***must return 0*** upon read back.
3. PC_BEEP default can be 0000h or 8000h, mute off or on.

6.3.1 Reset Register (Index 00h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	na

Writing any value to this register performs a register reset, which causes all registers to revert to their default values. Reading this register returns the ID code of the part and a code for the type of 3D Stereo Enhancement, if any.

All DACs operate at the same resolution. All ADCs operate at the same resolution. The possible exceptions are the modem ADC and DAC, ***which default to 16-bit resolution as described in AC ’97 2.0 Appendix B.*** Modem interoperability is not expected between AC `97 Controller / AC `97 pairs that aren't designed to work together, ***but vendor specific methods can be used to identify and support 18- or 20-bit resolution***. ***For example, an AC `97 Controller could determine the modem DAC/ADC resolution in an MC or AMC Codec by inspecting the vendor ID registers.***

AC ’97 2.1 annotation (originally published in the AC ’97 Technical FAQ, September 1996):
The standard AC ‘97 DAC and ADC resolutions are defined as 16-bits. 18- or 20-bit resolution implementations are optional. The audio driver for an “enhanced” AC ‘97 Controller can determine the implemented DAC and ADC resolution after it has been loaded by reading the AC ‘97 Codec’s Reset Register which is located at 0x00. If, for example, the driver has determined that the implemented DAC resolution is 16-bits yet the Controller supports 18- or 20-bit sample streams for playback, the Controller can either dither the sample streams down to 16-bits or pass the stream “as is”. Since all AC-link data time slots carry 20 bits, the non-dithered approach will result in the least significant bits which overrun the DAC width being dropped. For this reason dithering may be an attractive feature for the Controller that supports greater than 16-bit sample streams.

The ID decodes the capabilities of AC ‘97 based on the following:

Bit = 1	Function
ID0	Dedicated Mic PCM In channel
ID1	Reserved (was Modem Line Codec support)
ID2	Bass & Treble control
ID3	Simulated Stereo (Mono to Stereo)
ID4	Headphone out support
ID5	Loudness (bass boost) support
ID6	18 bit DAC resolution
ID7	20 bit DAC resolution
ID8	18 bit ADC resolution
ID9	20 bit ADC resolution

Table 8. Baseline Audio Optional Feature IDs

The 3D stereo enhancement decodes are based on Table 9. 3D Stereo Enhancement Vendor IDs. Note that the 3D control register defines two 16-step controls for the 3D Stereo Enhancement function. These controls can be used to support center and depth, but can also be used generically. The 3D control register should be read to determine if the selected enhancement is either fixed or variable center and depth. If the lower 8-bits of the 3D control register are non-zero, then the depth/generic1 control is fixed, otherwise it is variable. If the upper 8-bits of the 3D control register are non-zero, then the center/generic2 control is fixed, otherwise it is variable.

SE4...SE0	3D Stereo Enhancement Technique	SE4...SE0	3D Stereo Enhancement Technique
00000 (0)	No 3D Stereo Enhancement	01110 (14)	Binaura* 3D Audio Enhamcement
00001 (1)	Analog Devices* Phat Stereo	01111 (15)	ESS Technology* (stereo enhancement)
00010 (2)	Creative Stereo Enhancement	10000 (16)	Harman International* VMAx
00011 (3)	National Semi* 3D Stereo Enhancement	10001 (17)	Nvidea* 3D Stereo Enhancement
00100 (4)	YAMAHA* Ymersion	10010 (18)	Philips* Incredible Sound
00101 (5)	BBE* 3D Stereo Enhancement	10011 (19)	Texas Instruments* 3D Stereo Enhancement
00110 (6)	Crystal Semi* 3D Stereo Enhancement	10100 (20)	VLSI Technology* 3D Stereo Enhancement
00111 (7)	Qsound* QXpander	10101 (21)	TriTech* 3D Stereo Enhancement
01000 (8)	Spatializer* 3D Stereo Enhancement	10110 (22)	Realtek* 3D Stereo Enhancement
01001 (9)	SRS* 3D Stereo Enhancement	10111 (23)	Samsung* 3D Stereo Enhancement
01010 (10)	Platform Tech* 3D Stereo Enhancement	11000 (24)	Wolfson* Microelectronics 3D Enhancement
01011 (11)	AKM* 3D Audio	11001 (25)	Delta Integration* 3D Enhancement
01100 (12)	Aureal* Stereo Enhancement	11010 (26)	SigmaTel* 3D Enhacement
01101 (13)	AZTECH* 3D ENHANCEMENT	11100 (28)	Rockwell* 3D Stereo Enhancement

Table 9. 3D Stereo Enhancement Vendor IDs

6.3.2 Play Master Volume Registers (Index 02h, 04h and 06h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
02h	Master Volume	Mute	X	*ML5*	ML4	ML3	ML2	ML1	ML0	X	X	*MR5*	MR4	MR3	MR2	MR1	MR0	8000h
04h	*Headphone Volume*	*Mute*	*X*	*ML5*	*ML4*	*ML3*	*ML2*	*ML1*	*ML0*	*X*	*X*	*MR5*	*MR4*	*MR3*	*MR2*	*MR1*	*MR0*	*8000h*
06h	*Master Volume Mono*	*Mute*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*MM5*	*MM4*	*MM3*	*MM2*	*MM1*	*MM0*	*8000h*

These registers manage the output signal volumes. **Register 02h** controls the stereo master volume (both right and left channels), **Register 04h** controls the optional headphone volume or ***True Line Level volume as described in AC '97 2.1 Appendix D*** out. **Register 06h** controls the mono volume output, ***which is now optional as described in AC '97 2.1 Appendix D***. Each step corresponds to 1.5 dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞ dB. ML5 through ML0 is for the left channel level, MR5 through MR0 is for the right channel and MM5 through MM0 is for the mono out channel.

Support for the MSB of the level is optional. **If the MSB is not supported then AC '97 needs to detect when that bit is set and set all four LSBs to 1s.** Example: If AC '97 only supports 5 bits of resolution in its mixer and the driver writes a 1xxxxx AC '97 must interpret that as x11111. It will also respond when read with x11111 rather then 1xxxxx, the value writen to it. The driver can use this feature to detect if support for the 6th bit is there or not.

The default value is 8000h (1000 0000 0000 0000), which corresponds to 0 dB attenuation with mute on.

Mute	M*x*5...M*x*0	Function	Range
0	00 0000	0 dB Attenuation	Req.
0	01 1111	46.5dB Attenuation	Req.
0	11 1111	94.5dB Attenuation	Optional
1	xx xxxx	∞ dB Attenuation	Req.

Table 10. Master, Headphone, and Mono Volume

6.3.3 Master Tone Control Registers (Index 08h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
08h	*Master tone (R & L)*	*X*	*X*	*X*	*X*	*BA3*	*BA2*	*BA1*	*BA0*	*X*	*X*	*X*	*X*	*TR3*	*TR2*	*TR1*	*TR0*	*0F0Fh*

Optional register for support of tone controls (bass and treble). If the part does not support bass and treble, writing to this register will have no effect and reading will result in all don't care values. The step size is 3 dB with optional support for 1.5 dB. The step size option is accomplished by either using 3 bits (MSB justified) for 3 dB steps or all 4 bits for 1.5 dB steps. Writing a 0000h corresponds to +10.5 dB of gain. Center frequencies (from which gains are measured) are 100Hz for Bass and 10,000Hz for Treble. The default value is 0F0Fh, which corresponds to bypass of bass or treble gain.

TR3...*TR0* or BA3...*BA0*	Req support	Function
000*0*	yes	+10.5 dB of gain
000*1*	no	+9 dB of gain
001*0*	yes	+7.5 dB of gain
001*1*	no	+6 dB of gain
..		...
011*0*	yes	+1.5 dB of gain
011*1*	yes	0 dB of gain
100*0*	yes	-1.5 dB of gain
..		...
110*0*	yes	-7.5 dB
110*1*	no	-9 dB of gain
111*0*	yes	-10.5 dB of gain
111*1*	yes	Bypass

Table 11. Tone Control

6.3.4 PC Beep Register (Index 0Ah)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0Ah	*PC_BEEP Volume*	*Mute*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*PV3*	*PV2*	*PV1*	*PV0*	*X*	*x000h*

This controls the level for the PC Beep input, ***now optional as described in AC '97 2.1 Appendix D***. Each step corresponds to approximately 3 dB of attenuation. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞ dB.

PC_BEEP supports motherboard AC '97 Controller /Codec implementations. The intention of routing PC_BEEP through the Codec analog mixer is to eliminate the requirement for an onboard speaker or piezoelectric device by guaranteeing a connection to speakers connected via the output jack. In order for this to be viable the PC_BEEP signal needs to reach the output jack at all times, with or without the audio driver's support.

NOTE: The PC_BEEP is recommended to be routed to L & R Line outputs even when AC '97 is in a RESET State. This is so that Power On Self Test (POST) codes can be heard by the user in case of a hardware problem with the PC. This can be accomplished with a high impedance path to the outputs without any attenuation. For further PC_BEEP implementation details please refer to the AC '97 Technical FAQ sheet.

The default value can be 0000h or 8000h, which corresponds to 0 dB attenuation with mute off or on.

Mute	PV3...PV0	Function
0	0000	0 dB Attenuation
0	1111	45 dB Attenuation
1	xxxx	∞ dB Attenuation

Table 12. PC BEEP Volume

See AC '97 2.1 Appendix D for additional discussion of PC_BEEP implementations.

6.3.5 Analog Mixer Input Gain Registers (Index 0Ch - 18h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0Ch	*Phone Volume*	*Mute*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*GN4*	*GN3*	*GN2*	*GN1*	*GN0*	*8008h*
0Eh	Mic Volume	Mute	X	X	X	X	X	X	X	X	20 dB	*X*	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line In Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
14h	*Video Volume*	*Mute*	*X*	*X*	*GL4*	*GL3*	*GL2*	*GL1*	*GL0*	*X*	*X*	*X*	*GR4*	*GR3*	*GR2*	*GR1*	*GR0*	*8808h*
16h	*Aux Volume*	*Mute*	*X*	*X*	*GL4*	*GL3*	*GL2*	*GL1*	*GL0*	*X*	*X*	*X*	*GR4*	*GR3*	*GR2*	*GR1*	*GR0*	*8808h*
18h	PCM Out Vol	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h

This controls the gain/attenuation for each of the analog inputs. Each step corresponds to approximately 1.5 dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞ dB.

- **Register 0Eh** (Mic Volume Register) has an extra bit that is for a 20 dB boost. When bit 6 is set to 1 the 20 dB boost is on. The default value is 8008, which corresponds to 0 dB gain with mute on.

The default value for the mono registers is 8008h, which corresponds to 0 dB gain with mute on. The default value for stereo registers is 8808h, which corresponds to 0 dB gain with mute on.

Mute	G*x*4...G*x*0	Function
0	00000	+12 dB gain
0	01000	0 dB gain
0	11111	-34.5 dB gain
1	xxxxx	–∞ dB gain

Table 13. Mixer Input Gain/Atten

6.3.6 Record Select Control Register (Index 1Ah)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ah	Record Select	X	X	X	X	X	SL2	SL1	SL0	X	X	X	X	X	SR2	SR1	SR0	0000h

Used to select the record source independently for right and left. See table for legend. ***Several of the analog mixer inputs are now optional as described in AC '97 2.1 Appendix D, selecting an unimplemented analog input has undefined results.***

The default value is 0000h, which corresponds to Mic in.

SR2...SR0	Right Record Source
0	Mic
1	CD In (R)
2	Video In (R)
3	Aux In (R)
4	Line In (R)
5	Stereo Mix (R)
6	Mono Mix
7	Phone

SL2...SL0	Left Record Source
0	Mic
1	CD In (L)
2	Video In (L)
3	Aux In (L)
4	Line In (L)
5	Stereo Mix (L)
6	Mono Mix
7	Phone

Table 14. Left, Right Record Select

6.3.7 Record Gain Registers (Index 1Ch and 1Eh)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ch	Record Gain	Mute	X	X	X	GL3	GL2	GL1	GL0	X	X	X	X	GR3	GR2	GR1	GR0	8000h
1Eh	*Record Gain Mic*	*Mute*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*GM3*	*GM2*	*GM1*	*GM0*	*8000h*

1Ch is for the stereo input and 1Eh is for the optional special purpose correlated audio mic channel. Each step corresponds to 1.5 dB. 22.5dB corresponds to 0F0Fh and 000Fh respectively. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel(s) is set at -∞ dB.

The default value is 8000h, which corresponds to 0 dB gain with mute on.

Mute	G*x*3...G*x*0	Function
0	1111	+22.5 dB gain
0	0000	0 dB gain
1	xxxxx	–∞ dB gain

Table 15. Record Gain/Atten

6.3.8 General Purpose Register (Index 20h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
20h	General Purpose	POP	ST	3D	LD	X	X	MIX	MS	LPBK	X	X	X	X	X	X	X	0000h

This register is used to control miscellaneous optional functions of the AC '97 component. Below is a summary of each bit and its function. The *POP* bit controls the optional PCM out 3D bypass path (the pre- and post-3D PCM out paths are mutually exclusive). The *MS* bit controls the optional mic selector. The Loudness (bass boost) bit is to control an optional loudness contour or "bass boost" function. The exact implementation of this is left up to the vendor. This register should be read before writing to generate a mask for only the bit(s) that need to be changed. The function default value is 0000h which is all off. The optional LPBK bit enables loopback of the ADC output to the DAC input without involving the AC-link, allowing for full system performance measurements.

Bit	Function
POP	*PCM out path & mute, 0 = pre 3D, 1 = post 3D*
ST	*Simulated Stereo Enhancement on/off 1 = on*
3D	*3D Stereo Enhancement on/off 1 = on*
LD	*Loudness (bass boost) on/off 1 = on*
X	*Reserved*
X	*Reserved*
MIX	*Mono output select 0=Mix, 1=Mic*
MS	*Mic select 0 = Mic1, 1= Mic2*
LPBK	*ADC/DAC loopback mode*

Table 16. General Purpose Bit Definitions

6.3.9 3D Control Register (Index 22h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
22h	3D Control	X	X	X	X	CR3	CR2	CR1	CR0	X	X	X	X	DP3	DP2	DP1	DP0	0000h

This optional register is used to control the center and/or depth of the 3D stereo enhancement function built into of the AC '97 component. Note this register should be read to indicate if the selected 3D stereo enhancement is of either fixed or variable center and depth. If this control register is non-zero then the enhancement is fixed. The register default value is either the fixed value or 0000h if it is variable. Linear or logarithmic implementation is acceptable, depending on the 3D technology (linear is shown below):

CR3...CR0 DP3...DP0	Center Depth
0	0%
1	6.67%
.	.
14	93.33%
15	100%

Table 17. 3D Control

6.3.10 Reserved (was Modem Sample Rate Register) (Index 24h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
24h	*Reserved*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*

AC '97 2.0 Appendix B completely re-defines interoperable modem support, and discourages the use of any modem functionality originally defined in AC '97 1.03 within register range 00-28h. Register register 24h was the modem sample rate register previously, but is now reserved.

6.3.11 Powerdown Control/Status Register (Index 26h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
26h	Powerdown Ctrl/Stat	EAPD	*PR6*	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	na

This read/write register is used to program powerdown states and monitor subsystem readiness. The lower half of this register is read only status, a 1 indicating that the subsection is "*ready*". *Ready* is defined as the subsection able to perform in its nominal state. When this register is written the bit values that come in on AC-link will have no effect on read only bits 0-7.

When the AC-link "Codec Ready" indicator bit (SDATA_IN slot 0, bit 15) is a 1 it indicates that the AC-link and AC '97 control and status registers are in a fully operational state. The AC '97 Controller must further probe this Powerdown Control/Status Register to determine exactly which subsections, if any, are ready.

Bit	Function
X	Reserved
REF	Vref's up to nominal level
ANL	Analog mixers, etc. ready
DAC	DAC section ready to accept data
ADC	ADC section ready to transmit data

Table 18. Baseline Powerdown Status bit Definitions

The power down modes are as follows. The first three bits are to be used individually rather than in combination with each other. The last bit PR3 can be used in combination with PR2 or by itself. PR0 and PR1 control the PCM ADC's and DAC's only, PR7 independently controls the optional modem ADC and DAC.

Bit	Function
PR0	PCM in ADC's & Input Mux Powerdown
PR1	PCM out DACs Powerdown
PR2	Analog Mixer powerdown (Vref still on)
PR3	Analog Mixer powerdown (Vref off)
PR4	Digital Interface (AC-link) powerdown (external clk off)
PR5	Internal Clk disable
PR6	*HP amp powerdown*
EAPD	***External Amplifier Power Down***

Table 19. Baseline Powerdown Control bit Definitions

6.3.12 Extended Audio Registers (Index 28h – 3Ah)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
28h-3Ah	*AC '97 2.0 Audio See Appendix A*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*

AC '97 2.0 Appendix A defines audio extensions using registers 28h – 3Ah.

6.3.13 Extended Modem Registers (Index 3Ch – 58h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
3Ch-58h	*AC '97 2.0 Modem See Appendix B*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*

AC '97 2.0 Appendix B defines modem extensions using registers 3Ch – 58h.

6.3.14 Vendor Reserved Registers (Index 5Ah - 7Ah)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
5Ah-7Ah	*Vendor Reserved*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*

These are reserved for future use and are vendor specific. Do not write to these registers unless the Vendor ID register has been checked first to ensure that the driver knows the source of the AC '97 component.

6.3.15 Vendor ID Registers (Index 7Ch - 7Eh)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	na
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	na

These registers are for specific vendor identification if so desired. The ID method is Microsoft's Plug and Play Vendor ID code with F7..0 the first character of that id, S7..0 the second character and T7..0 the third character. These three characters are ASCII encoded. The REV7..0 field is for the Vendor Revision number.

7. Low Power Modes

AC ‘97 can operate at reduced power when no activity is required. The state of power down is controlled by the Powerdown Register (26h). There are seven commands of separate power down with the addition of the Modem Codec. See Table 19 for the different modes. AC ‘97 is assumed to be a fully static design, that is if the clock is stopped the registers will not lose their values.

AC ’97 2.1 Appendix D provides extensive recommendations for power management of audio and modem devices.

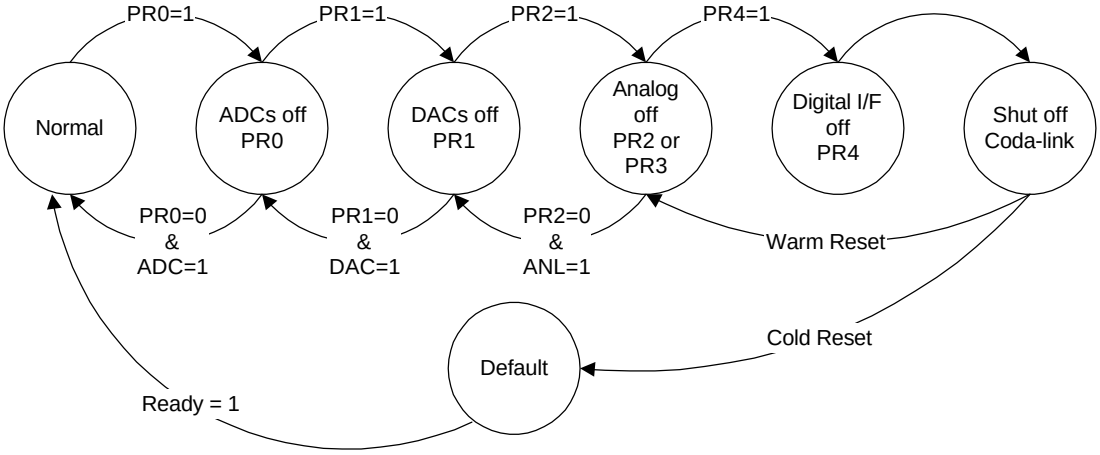


Figure 17. One example of AC ‘97 Powerdown/Powerup flow

Figure 17 illustrates one example procedure to do a complete powerdown of AC ‘97. From normal operation sequential writes to the Powerdown Register are performed to power down AC ‘97 a piece at a time. After everything has been shut off, a final write (of PR4) can be executed to shut down the AC ‘97’s digital interface (AC-link). The part will remain in sleep mode with all its registers holding their static values. To wake-up, the AC ‘97 Controller will send a pulse on the sync line issuing a warm reset. This will restart AC ‘97’s digital interface (resetting PR4 to zero). AC ‘97 can also be woken up with a cold reset. A cold reset will cause a loss of values of the registers as a cold reset will set them to their default states. When a section is powered back on the Powerdown Control/Status register (index 26h) should be read to verify that the section is ready (i.e. stable) before attempting any operation that requires it.

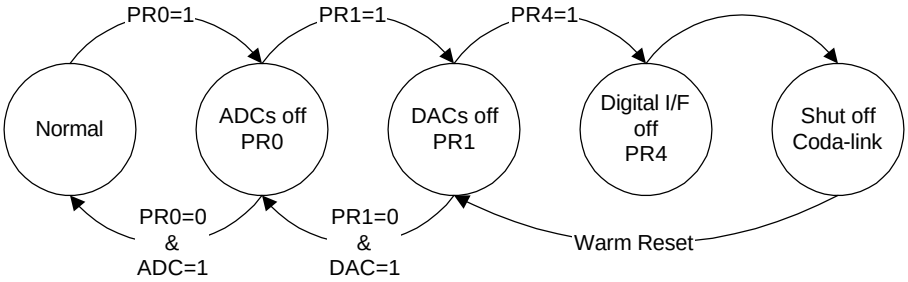


Figure 18. AC ‘97 Powerdown/Powerup flow with analog mixer still alive

Figure 18 illustrates a state when all the mixers should work with the static volume settings that are contained in their associated registers. This is used when the user could be playing a CD (or external LINE_IN source) through AC '97 to the speakers but have most of the system in low power mode. The procedure for this follows the previous except that the analog mixer is never shut down.

8. Testability

8.1 Activating the Test Modes

AC ‘97 has two test modes. One is for ATE in circuit test and the other is for vendor-specific tests. AC ‘97 enters the ATE in circuit test mode if SDATA_OUT is sampled high at the trailing edge of RESET#. AC ‘97 enters the vendor-specific test mode when coming out of RESET if SYNC is high. These cases will never occur during standard operating conditions.

Regardless of the test mode, the AC ‘97 Controller must issue a cold reset to resume normal operation of the AC ‘97 Codec.

8.2 Test Mode Functions

8.2.1 ATE in circuit test mode

When AC ‘97 is placed in the ATE test mode, its digital AC-link outputs (i.e. BIT_CLK and SDATA_IN) are driven to a high impedence state. This allows ATE in circuit testing of the AC ‘97 Controller.

8.2.2 Vendor-specific test mode

To be left up to the individual vendors.

9. AC-link Digital DC and AC Characteristics

AC '97 2.1 Appendix D updates DC and AC characteristics. Chapter 9 should NOT be used for new designs.

9.1 DC Characteristics

AC '97 2.1 Appendix D updates DC and AC characteristics. Chapter 9 should NOT be used for new designs.
($T_{ambient}$ = 25^{0}C, AVdd = DVdd = 5.0V or 3.3V +/- 5%; AVss = DVss = 0V; 50pF external load)

Parameter	Symbol	Min	Typ	Max	Units
Input voltage range	V_{in}	-0.30	-	DVdd + 0.30	V
Low level input voltage	V_{il}	-	-	0.30 x Vdd	V
High level input voltage	V_{ih}	0.40 x Vdd	-	-	V
High level output voltage	V_{oh}	0.50 x Vdd	-	-	V
Low level output voltage	V_{ol}	-	-	0.20 x Vdd	V
Input Leakage Current (AC-link inputs)	-	-10	-	10	uA
Output Leakage Current (Hi-Z'd AC-link outputs)	-	-10	-	10	uA
Output buffer drive current	-	-	5	-	mA

Table 20. DC Characteristics (relative to Vdd)

NOTE: It is recommended that the digital portion of the AC '97 component be capable of operating at either 5.0V or 3.3V (+/- 5%), depending on which DVdd is supplied (see section 3.4 for descriptions of Power and Ground Signal levels).

To specify operation of the digital portion of the AC '97 component at both 5.0 V and 3.3 V, the low and high level input and output voltages are specified as percentages of the digital supply voltage. The AC '97 Working Group believes that it is possible to deliver dual voltage parts which meet the above specification. However, the following has been added to simplify the implementation for those who do not support dual voltage (and possibly those who do), by allowing 5.0 or 3.3 V parts to match the PCI 2.1 specifications for V_{ih}, V_{il}, V_{oh}, and V_{ol}:

5.0 V Only Operation					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**
Input voltage range	V_{in}	-0.30	-	5.30	V
Low level input voltage	V_{il}	-	-	0.8	V
High level input voltage	V_{ih}	2.0	-	-	V
High level output voltage	V_{oh}	2.4	-	-	V
Low level output voltage	V_{ol}	-	-	.55	V

Table 21. DC Characteristics (5.0 V Operation as per PCI 2.1)

3.3 V Only Operation					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**
Input voltage range	V_{in}	-0.30	-	3.60	V
Low level input voltage	V_{il}	-	-	1.0	V
High level input voltage	V_{ih}	1.6	-	-	V
High level output voltage	V_{oh}	2.97	-	-	V
Low level output voltage	V_{ol}	-	-	0.33	V

Table 22. DC Characteristics (3.3 V Operation as per PCI 2.1)

9.2 AC Timing Characteristics

AC '97 2.1 Appendix D updates DC and AC characteristics. Chapter 9 should NOT be used for new designs.
($T_{ambient}$ = 25^0C, AVdd = DVdd = 5VDC or 3.3VDC; AVss = DVss = 0V; 50pF external load)

9.2.1 Reset

AC '97 2.1 Appendix D updates DC and AC characteristics. Chapter 9 should NOT be used for new designs.

9.2.1.1 Cold Reset

AC '97 2.1 Appendix D updates DC and AC characteristics. Chapter 9 should NOT be used for new designs.

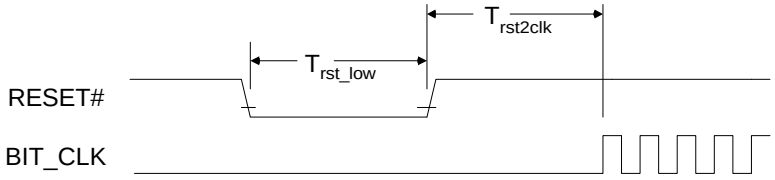


Figure 19. Cold Reset timing diagram

Parameter	Symbol	Min	Typ	Max	Units
RESET# active low pulse width	T_{rst_low}	1.0	-	-	us
RESET# inactive to BIT_CLK startup delay	$T_{rst2clk}$	162.8	-	-	ns

Table 23. Cold Reset timing parameters

9.2.1.2 Warm Reset

AC '97 2.1 Appendix D updates DC and AC characteristics. Chapter 9 should NOT be used for new designs.

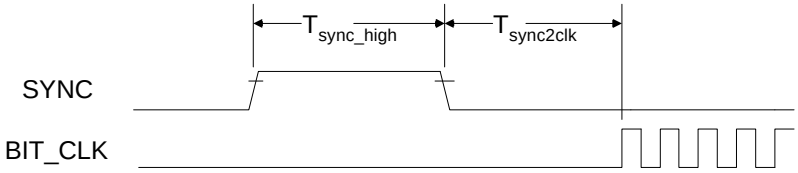


Figure 20. Warm Reset timing diagram

Parameter	Symbol	Min	Typ	Max	Units
SYNC active high pulse width	T_{sync_high}	-	1.3	-	us
SYNC inactive to BIT_CLK startup delay	$T_{sync2clk}$	162.8	-	-	ns

Table 24. Warm Reset timing parameters

9.2.2 Clocks

AC '97 2.1 Appendix D updates DC and AC characteristics. Chapter 9 should NOT be used for new designs.

(50pF external load)

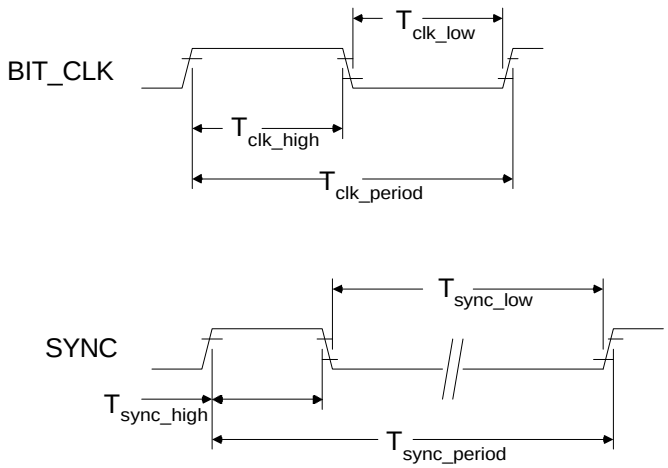


Figure 21. BIT_CLK to SYNC timing diagram

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	T_{clk_period}	-	81.4	-	ns
BIT_CLK output jitter		-	-	750	ps
BIT_CLK high pulse width (note 1)	T_{clk_high}	32.56	40.7	48.84	ns
BIT_CLK low pulse width (note 1)	T_{clk_low}	32.56	40.7	48.84	ns
SYNC frequency		-	48.0	-	kHz
SYNC period	T_{sync_period}	-	20.8	-	us
SYNC high pulse width	T_{sync_high}	-	1.3	-	us
SYNC low pulse width	T_{sync_low}	-	19.5	-	us

Table 25. BIT_CLK to SYNC timing parameters

Notes:
1) Worst case duty cycle restricted to 40/60.

9.2.3 Data Setup And Hold

AC '97 2.1 Appendix D updates DC and AC characteristics. Chapter 9 should NOT be used for new designs.

(50pF external load)

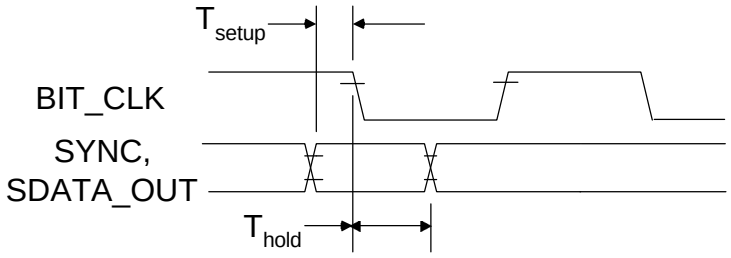


Figure 22. Data setup and hold timing diagram

Parameter	Symbol	Min	Typ	Max	Units
Setup to falling edge of BIT_CLK	T_{setup}	15.0	-	-	ns
Hold from falling edge of BIT_CLK	T_{hold}	5.0	-	-	ns

Table 26. Data setup and hold timing parameters

Note 1: Setup and hold time parameters for SDATA_IN are with respect to the AC '97 Controller.

9.2.4 Signal Rise and Fall Times

AC '97 2.1 Appendix D updates DC and AC characteristics. Chapter 9 should NOT be used for new designs.
(50pF external load; from 10% to 90% of Vdd)

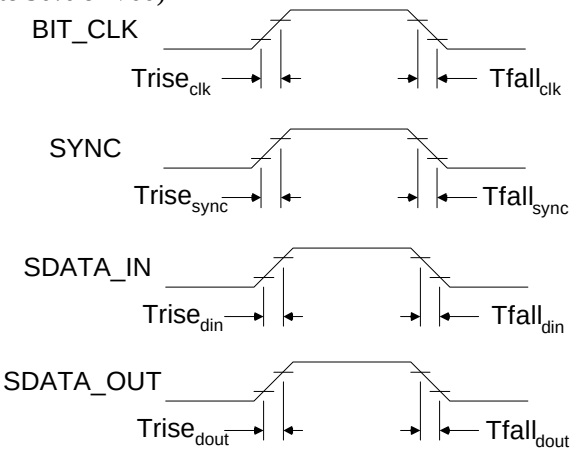


Figure 23. Signal rise and fall times diagram

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK rise time	$Trise_{clk}$	2	-	6	ns
BIT_CLK fall time	$Tfall_{clk}$	2	-	6	ns
SYNC rise time	$Trise_{sync}$	2	-	6	ns
SYNC fall time	$Tfall_{sync}$	2	-	6	ns
SDATA_IN rise time	$Trise_{din}$	2	-	6	ns
SDATA_IN fall time	$Tfall_{din}$	2	-	6	ns
SDATA_OUT rise time	$Trise_{dout}$	2	-	6	ns
SDATA_OUT fall time	$Tfall_{dout}$	2	-	6	ns

Table 27. Signal rise and fall times parameters

9.2.5 AC-link Low Power Mode Timing

AC ’97 2.1 Appendix D updates DC and AC characteristics. Chapter 9 should NOT be used for new designs.

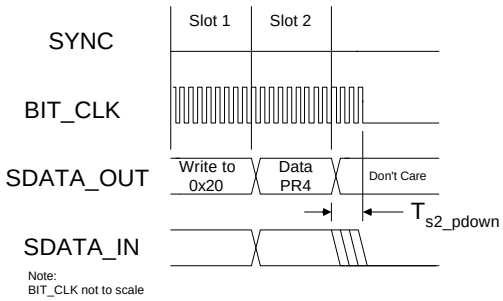


Figure 24. AC-link low power mode timing diagram

Parameter	Symbol	Min	Typ	Max	Units
End of Slot 2 to BIT_CLK, SDATA_IN low	T_{s2_pdown}	-	-	1.0	us

Table 28. AC-link low power mode timing parameters

9.2.6 ATE Test Mode

AC ’97 2.1 Appendix D updates DC and AC characteristics. Chapter 9 should NOT be used for new designs.

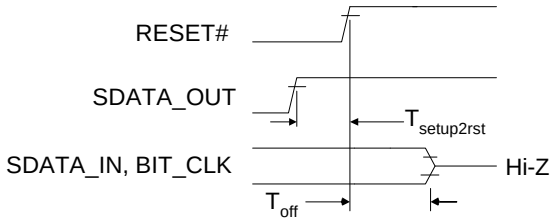


Figure 25. ATE test mode timing diagram

Parameter	Symbol	Min	Typ	Max	Units
Setup to trailing edge of RESET# (also applies to SYNC)	T_{off}	15.0	-	-	ns
Rising edge of RESET# to Hi-Z delay	T_{off}	-	-	25.0	ns

Table 29. ATE test mode timing parameters

Notes:

1. All AC-link signals are normally low through the trailing edge of RESET#. Bringing SDATA_OUT high for the trailing edge of RESET# causes AC ‘97’s AC-link outputs to go high impedance which is suitable for ATE in circuit testing.

2. A vendor-specific internal test mode can be entered by bringing SYNC high for the trailing edge of RESET#. This mode has no effect on AC ‘97 AC-link output signal levels.

3. Once either of the two test modes have been entered, AC ‘97 must be issued another RESET# with all AC-link signals low to return to the normal operating mode.

10. Analog Performance Characteristics

(Standard test conditions unless otherwise noted: $T_{ambient}$ = 25^{0}C; DVdd = 5.0 or 3.3 V +/- 5%; AVdd = 5.0 V +/- 5%; Input Voltage Levels: Logic Low = 0.35*Vdd, Logic High = 0.65*Vdd; 1 kHz input sine wave; Sample Frequency = 48 kHz; 0 dB = 1Vrms, 10KΩ/50pF load, Testbench Characterization BW: 20 Hz – 20 kHz, 0 dB attenuation; tone and 3D disabled)

Parameter	Min	Typ	Max	Units
Full Scale Input Voltage:				
Line Inputs	-	1.0	-	Vrms
Mic Inputs[1]	-	0.1	-	
Full Scale Output Voltage:	-	-	-	
Line Output	-	1.0	-	Vrms
Headphone Output	-	-	1.41	
Analog S/N:				
CD to LINE_OUT	90	-	-	dB
Other to LINE_OUT	-	85	-	
Analog Frequency Response[2]	20	-	20,000	Hz
Digital S/N[3]				
D/A	85	90	-	dB
A/D	75	80	-	
Total Harmonic Distortion:				
Line Output[4]	-	-	0.02	%
Headphone Output[5]	-	-	1.0	
D/A & A/D Frequency Response[6]	20	-	19,200	Hz
Transistion Band	19,200	-	28,800	Hz
Stop Band	28,800	-	∞	Hz
Stop Band Rejection[7]	-74	-	-	dB
Out-of-Band Rejection[8]	-	-40	-	dB
Group Delay	-	-	1	ms
Power Supply Rejection Ratio (1 kHz)	-	-40	-	dB
Crosstalk between Inputs channels	-	-	-70	dB
Spurious Tone Reduction	-	-100	-	dB
Attenuation, Gain Step Size[9]	-	1.5	-	dB
Input Impedance	10	-	-	kOhm
Input Capacitance	-	7.5	-	pF
Vrefout	-	2.25-2.75	-	V

Table 30. AC '97 analog performance characteristics

Notes:

(1) With +20 dB Boost on, 1.0 Vrms with Boost off

(2) ±1dB limits

(3) The ratio of the rms output level with 1kHz full scale input to the rms output level with all zeros into the digital input. Measured "A wtd" over a 20 Hz to a 20 kHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).

(4) 0 dB gain, 20 kHz BW, 48 kHz Sample Frequency

(5) +3 dB output into 32Ω load

(6) ±0.25 dB limits

(7) Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.

(8) The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 kHz, with respect to a 1VRMS DAC output.

(9) Gain step size 1.5 dB is true for all attenuators except for PC_BEEP, which has 3.0dB step size.

11. AC ’97 2.0 Extensions

AC ’97 2.1 Appendix D also includes additions or clarifications for audio, modem, and multiple Codec implementations.

11.1 Introduction

In response to requests from audio and modem IHVs as well as PC OEMs, Intel invited Audio Codec ’97 licensees to participate in a Working Group to extend the AC '97 Component Specification to include interoperable definitions for the following functionality:

Appendix A: AC ’97 2.0 Variable Sample Rate Extension
Appendix B: AC ’97 2.0 Modem AFE Extension
Appendix C: AC ’97 2.0 Multiple Codec Extension

All of the extensions are defined as optional Appendices to the current AC '97 Component Specification, and are intended to enable future generations of interoperable AC-link-based audio and modem Codecs and Controllers. As with AC '97, the intention is to define a common interoperable high-level feature set, yet provide flexibility for actual implementation. An Extended AC ’97 2.0 Register Summary is provided at the end of the introduction section**.**

The AC ’97 extensions are designed to allow one commonly defined Digital Controller (also referred to as DC ’97) to target a variety of AC-link functionality implemented as

- audio only with existing AC ’97 Codec
- audio only with extended AC ’97 Codec (also referred to as AC ’97 2.0)
- a combo audio modem Codec (also referred to as AMC ’97)
- separate Codecs for audio (AC ’97 2.0) and modem (also referred to as MC ’97)
- dual Codecs for mobile (AC ’97, AC ’97 2.0, or AMC ’97) and dock (AC ’97 or AC ’97 2.0)
- multiple Codecs (one primary and up to three secondary)

In addition, the 2-channel extended AC ’97 2.0 audio functionality has been defined to be backward-compatible with current AC ’97 Controllers.

11.2 Overview of Extended AC ’97 2.0 Functionality

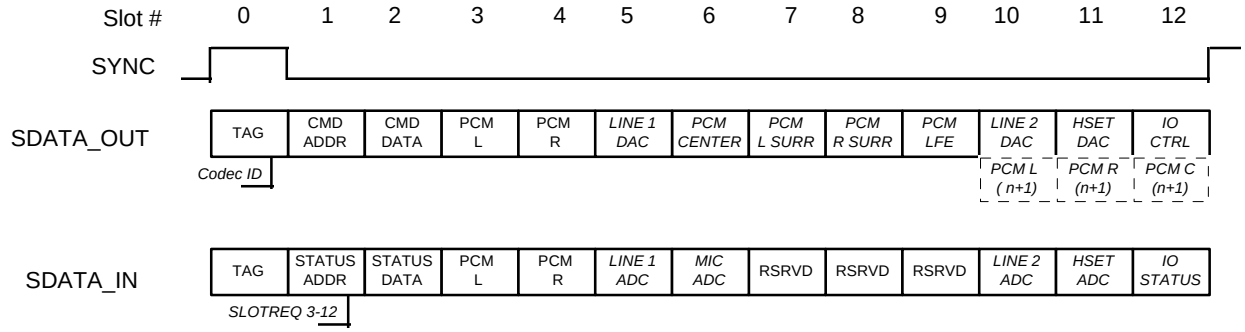


Figure 26. Extended AC ’97 2.0 Slot Definitions

11.2.1 AC ’97 2.0 Audio

Optional multi-channel audio (*CENTER, L and R SURROUND, LFE*) assignments for AC-link output slots 6-9 were introduced last year in the AC ’97 FAQ paper, and are included here. Note that the market for 6-channel analog output may be limited to the PC Theater segment and special purpose add-in cards. The majority of PCs with

DVD drives are expected to offer matrix-encoded stereo analog output as well as digital multi-channel output via S/P-DIF, USB, or IEEE 1394.

Optional variable sample rate audio extends the AC '97 architecture to address host-based solutions, similar to those appearing on USB, by minimizing the sample rate conversion (SRC) burden (at least for the initial audio stream). High quality digital SRC and mixing support for both 44.1 and 48 kHz content remain key requirements for supporting multiple audio sources, regardless of Controller architecture (host-based or hardware-accelerated Controllers).

Variable sample rate operation is supported via newly-defined sample rate control registers for audio DAC and ADC groups and dedicated SLOTREQ bits in the previously unused LSBs (trailing bits) of input slot 1. If variable sample rate output is supported, the AC '97 2.0 Codec examines its audio sample rate control registers, the state of its FIFOs, and the incoming SDATA_OUT tag bits at the beginning of each audio output frame to determine which SLOTREQ bits to set active. SLOTREQ bits asserted during the current audio input frame indicate which output slots require data from the AC '97 Digital Controller in the next audio output frame. For fixed 48 kHz sample rate operation the SLOTREQ bits are always set active and a sample is transferred each frame. If variable sample rate input is supported, the tag bit for each input slot indicates whether valid data is present or not.

***Optional double-rate audio output*.** Support is defined for optional 88.2 or 96 kHz DAC operation, but implementation is not recommended at this time. Current DVD implementations for CE and PCs allow 96 kHz audio to be down-sampled to 48 kHz for high quality rendering. However, should higher sample rate audio become a requirement for DVD compatibility, output slots 10-12 have been assigned as optional *n+1* sample carriers in order to enable double-rate operation on front (L, C, and R) DAC channels with up to 20-bits (120 dB dynamic range) at 88.2 or 96 kHz.

True line level out. It is recommended that new AC '97 Codecs support a true consumer equipment-compatible (10 K Ohm) line level output that does not change with master volume settings. Built-in (as opposed to external) 32-Ohm headphone drive for the optional HP_OUT has not been widely implemented due to power dissipation limitations of the 48-pin and 64-pin packages selected for AC '97. It is therefore recommended that headphone drive (if required) be kept external to the Codec, and driven from the same master output that drives the speakers. By redefining HP_OUT as LNLVL_OUT and using the independent volume controls in register 04h, LNLVL_OUT can be set once to provide a fixed 1V RMS (2.8 V peak-to-peak) output level for a 0 dB gain PCM output stream. The optional HP_OUT Common pin is no longer needed, and may be used as a cap or ground pin. Also, 5 V analog (AVdd) operation is preferred to 3.3V, because of the potential impact 3.3 V operation will have on line output levels and SNR.

A 2-channel AC '97 2.0 Codec configured to default to fixed 48 kHz operation should be backward-compatible with current AC '97 Digital Controllers.

The 48-pin package and pin out for the AC '97 Codec has been widely accepted, and continues to be a recommendation for AC '97 2.0 audio.

11.2.2 AMC '97 2.0 Combined Audio and Modem AFE

Defined support for modem AFE now includes output and input slot assignments for two lines, a handset, up to 16 GPIO control bits, variable sample rate operation, and wake-up event signaling protocols.

Similar to the AC '97 2.0 audio case, but required for modem, variable sample rate operation is supported via a newly-defined modem sample rate control register for each modem DAC/ADC pair and dedicated SLOTREQ bits in the previously unused LSBs (trailing bits) of input slot 1.

For variable sample rate output, the AMC '97 Codec examines its audio and modem sample rate control registers, the state of its FIFOs, and the incoming SDATA_OUT tag bits at the beginning of each audio output frame to determine which SLOTREQ bits to set active. SLOTREQ bits asserted during the current audio input frame signal which output slots require data from the AC '97 Digital Controller in the next audio output frame.

For variable sample rate input, the tag bit for each input slot indicates whether valid data is present or not.

In order to allow freedom for optimal implementation of AMC ’97 combined audio and modem AFE functionality, these extensions focus exclusively on AC-link interoperability. Package and pin out are left to the individual vendor.

11.2.3 MC ’97 2.0 Modem AFE

The multiple Codec extension detailed in Appendix C defines the basic support needed to separate the modem AFE functionality from the audio yet allow a single AC ’97 Digital Controller to operate with both devices. Key requirements for a such implementations are that all AC-link devices operate synchronously from a common clock, that the audio and modem AFE register spaces be well defined, and that the AC ’97 Digital Controller support two SDATA_IN inputs, one for the primary Codec (AC ’97 1.0 or 2.0) and one for a secondary Codec (MC ’97).

In order to allow freedom for optimal implementation of MC ’97 modem AFE functionality, these extensions focus exclusively on AC-link interoperability. Package and pin out are left to the individual vendor.

11.3 Extended AC '97 2.0 Register Summary

The AC '97 Register space supports 64 16-bit registers using even 7-bit addresses. In the original AC '97 Component Specification locations 0h - 26h were allocated to specific AC '97 functionality, locations 28h - 58h were reserved for future use, and locations 5Ah - 7E were allocated to vendor-specific functionality. For AC '97 Extensions many of the 25 previously-reserved registers from 28h - 58h have been assigned in support of AC/AMC/MC '97 audio and modem AFE functionality.

All reserved bits (marked x) should be read as zero, and zeros should be written to these bits by Controllers and software. AC '97 2.0 Codecs should ~~ignore~~ ***respond with 0*** to accesses of odd-numbered registers instead of aliasing them to the next lower even-numbered register. As a result, odd-numbered registers can be reserved for future expansion.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
28h	Extended Audio ID	ID1	ID0	x	x	x	x	AMAP	LDAC	SDAC	CDAC	x	x	VRM	x	DRA	VRA	xxxxh
2Ah	Ext'd audio Stat/Ctrl	x	PRL	PRK	PRJ	PRI	x	MADC	LDAC	SDAC	CDAC	x	x	VRM	x	DRA	VRA	xxxxh
2Ch	PCM Front DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
2Eh	PCM Surround DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
30h	PCM LFE DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
32h	PCM LR ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
34h	MIC ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
36h	6CH Vol: C, LFE	mute	x	*LFE5*	LFE4	LFE3	LFE2	LFE1	LFE0	mute	x	*CNT5*	CNT4	CNT3	CNT2	CNT1	CNT0	8080h
38h	6CH Vol: L, R Surr	mute	x	*LSR5*	LSR4	LSR3	LSR2	LSR1	LSR0	mute	x	*RSR5*	RSR4	RSR3	RSR2	RSR1	RSR0	8080h
3Ah	RESERVED	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
3Ch	Extended Modem ID	ID1	ID0	x	x	x	x	x	x	x	x	x	CID2	CID1	HSET	LIN2	LIN1	xxxxh
3Eh	Ext'd Modem Stat/Ctrl	PRH	PRG	PRF	PRE	PRD	PRC	PRB	PRA	HDAC	HADC	DAC2	ADC2	DAC1	ADC1	MREF	GPIO	xxxxh
40h	Line 1 DAC/ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
42h	Line 2 DAC/ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
44h	Handset DAC/ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
46h	Line 1 DAC/ADC level	mute	x	x	x	DAC3	DAC2	DAC1	DAC0	mute	x	x	x	ADC3	ADC2	ADC1	ADC0	8080h
48h	Line 2 DAC/ADC level	mute	x	x	x	DAC3	DAC2	DAC1	DAC0	mute	x	x	x	ADC3	ADC2	ADC1	ADC0	8080h
4Ah	Handset DAC/ADC level	mute	x	x	x	DAC3	DAC2	DAC1	DAC0	mute	x	x	x	ADC3	ADC2	ADC1	ADC0	8080h
4Ch	GPIO Pin Config	GC15	GC14	GC13	GC12	GC11	GC10	GC9	GC8	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	xxxxh
4Eh	GPIO Pin Polarity/Type	GP15	GP14	GP13	GP12	GP11	GP10	GP9	GP8	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	FFFFh
50h	GPIO Pin Sticky	GS15	GS14	GS13	GS12	GS11	GS10	GS9	GS8	GS7	GS6	GS5	GS4	GS3	GS2	GS1	GS0	0000h
52h	GPIO Pin Wake up	GW15	GW14	GW13	GW12	GW11	GW10	GW9	GW8	GW7	GW6	GW5	GW4	GW3	GW2	GW1	GW0	0000h
54h	GPIO Pin Status	GI15	GI14	GI13	GI12	GI11	GI10	GI9	GI8	GI7	GI6	GI5	GI4	GI3	GI2	GI1	GI0	xxxxh
56h	Misc Mdm AFE Stat/Ctrl	CID2	CID1	CIDR	MLNK	x	HSB2	HSB1	HSB0	x	L2B2	L2B1	L2B0	x	L1B2	L1B1	L1B0	x000h
58h	RESERVED	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Table 31. Extended AC '97 Register Map

Appendix A. AC '97 2.0 Variable Sample Rate Extension

A.1 Introduction

The AC-link serial interconnect defines a digital data and control pipe between the Controller and the Codec. The AC-link supports 12 20-bit slots at 48 kHz on SDATA_IN and SDATA_OUT. The time division multiplexed (TDM) "slot-based" architecture supports a per-slot valid tag infrastructure that the source of each slot's data sets or clears to indicate the validity of the slot data within the current audio frame.

The AC-link's tag infrastructure can be used to support transfers between Controller and Codec at any sample rate. If desired, streams can be sent across the AC-link in a negotiated, "tag interleaved" fashion, thereby eliminating the need for up-sampling to a common rate such as 48 kHz.

For audio, optional AC-link slot interleaved solutions enable the stream of the highest intended quality, either 44.1 or 48 kHz, to be sent along the AC-link with no up-sampling required. Double-rate audio output at 88.2 or 96 kHz, should it become a requirement, can be supported by combining two output slots per DAC channel. For modem AFE, data streams at a variety of required sample rates can be supported.

The purpose of this extension is to define an interoperable, backward-compatible (with current AC '97 Digital Controllers) method for transferring data streams at rates other than 48 kHz across the AC-link. This includes the following definitions:

- Extended audio register definitions
- Audio sample rate control register definitions
- "On demand" sample transport scheme definitions

A.2 Extended Audio Register Definitions

The following newly-defined registers support variable sample rate audio output and input, double-rate audio output, and multi-channel audio output.

A.2.1 Extended Audio ID Register (Index 28h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
28h	Extended Audio ID	ID1	ID0	x	x	x	x	AMAP	LDAC	SDAC	CDAC	x	x	VRM	x	DRA	VRA	xxxxh

The Extended Audio ID is a *read only* register that identifies which extended audio features are supported (in addition to the original AC '97 features identified by reading the Reset register at Index 0h). A non-zero Extended Audio ID value indicates one or more of the extended audio features are supported.

- VRA=1 indicates optional Variable Rate PCM Audio is supported (PCM rates, as per Table 32)
- DRA=1 indicates optional Double-Rate PCM Audio output is supported
- VRM=1 indicates optional Variable Rate MIC input is supported (MIC rates as per Table 32)
- CDAC=1 indicates optional PCM Center DAC is supported
- SDAC=1 indicates optional PCM Surround DAC is supported
- LDAC=1 indicates optional PCM LFE DAC is supported
- ***AMAP=1 indicates optional slot/DAC mappings based on Codec ID (Refer to AC'97 2.1 Appendix D for description)***
- ID1, ID0 is a 2-bit field which indicates the Codec configuration: Primary is 00; Secondary is 01, 10, or 11 (see Appendix C for details)

If optional Variable Rate Audio is supported by the Codec, the AC '97 Digital Controller can further identify the specific capabilities of each DAC/ADC group by enabling VRA mode (VRA=1 in the Extended Audio Status and Control register) and writing and reading values to/from the associated sample rate control registers (defined below).

The value after cold or ~~warm~~ register reset for this register is constant, and depends on the features supported and the hardware configuration as Primary or Secondary Codec.

A.2.2 Extended Audio Status and Control Register (Index 2Ah)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
2Ah	Ext'd audio Stat/Ctrl	x	PRL	PRK	PRJ	PRI	x	MADC	LDAC	SDAC	CDAC	x	x	VRM	x	DRA	VRA	xxxxh

The Extended Audio Status and Control Register is a *read/write* register that provides status and control of the extended audio features.

Bits D3-D0 are *read/write* controls that enable or disable the extended audio features
- VRA=1 enables Variable Rate Audio mode (sample rate control registers and SLOTREQ signaling)
- DRA=1 enables Double-Rate Audio mode
- VRM=1 enables Variable Rate Audio mode for the dedicated MIC ADC

Bits D9-D6 are *read only* status of the extended audio feature readiness
- CDAC=1 indicates the PCM Center DAC is ready (6CH mode)
- SDAC=1 indicates the PCM Surround DACs are ready (6CH mode)
- LDAC=1 indicates the PCM LFE DAC is ready (6CH mode)
- MADC=1 indicates the MIC ADC is ready (new status for previously-defined AC '97 feature)

Bits D14-D11 are *read/write* controls of the extended audio feature powerdown
- PRI=1 turns the PCM Center DAC off
- PRJ=1 turns the PCM Surround DACs off (6CH mode)
- PRK=1 turns the PCM LFE DACs off (6CH mode)
- PRL=1 turns the MIC ADC off (MIC ADC operation is independent of PR0 from 26h)

The default value after cold or ~~warm~~ register reset for this register (xxxxh) is all extended features disabled (D3-D0 =0) and powered down (D14-D11=1). The feature readiness status should always be accurate (D9-D6=x).

A.2.3 Audio Sample Rate Control Registers (Index 2Ch - 34h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
2Ch	PCM Front DAC rate (output slots 3, 4, 6)	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
2Eh	PCM Surr DAC rate (output slots 7, 8)	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
30h	PCM LFE DAC rate (output slot 9)	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
32h	PCM LR ADC rate (input slots 3, 4)	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
34h	MIC ADC rate (input slot 5)	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

For audio, groups of DACs and ADCs are governed by read/write sample rate control registers that contain 16-bit unsigned values between 0 and 65535, representing the rate of operation in Hz. In VRA mode, if the value written to the register is supported that value will be echoed back when read, otherwise the closest (higher in case of a tie) sample rate supported is returned. It is desirable, but not required, that PCM DAC and ADC groups be capable of

operating at independent rates, otherwise a currently active DAC or ADC rate may limit availability of the associated converter.

If the optional Double Rate Audio (DRA) mode is active, the sample rate programmed will be multiplied by 2x. For example: When running at 88.2 kHz, the DRA bit will be programmed to 1, and the sample rate programmed would be 44,100.

If optional Variable Rate Audio is implemented, the minimum requirement is dual-rate operation at either 44.1 or 48 kHz, with additional support for 8.0, 11.025, 16, and 22.05 kHz recommended until the WDM audio architecture is firmly established, and Windows 3.11 and Windows 95 support are not also required.

Required (√) and *recommended (+)* sample rates for Variable Rate Audio (Hz)				
Sample rate	**D15-D0**	**PCM out**	**PCM in**	**Opt Mic**
8000	*1F40*	+	+	√
11025	*2B11*	+	+	
16000	*3E80*	+	+	√
22050	*5622*	+	+	
44100	**AC44**	√	√	
48000	**BB80**	√	√	√

Table 32. Sample Rates for Variable Rate Audio (Hz)

The default value after cold or ~~warm~~ register reset for these registers (BB80h) is 48 kHz.

A.2.4 6-Channel Volume Control Register (Index 36h and 38h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
36h	6CH Vol: C, LFE	mute	x	*LFE5*	LFE4	LFE3	LFE2	LFE1	LFE0	mute	x	*CNT5*	CNT4	CNT3	CNT2	CNT1	CNT0	8080h
38h	6CH Vol: L, R Surr	mute	x	*LSR5*	LSR4	LSR3	LSR2	LSR1	LSR0	mute	x	*RSR5*	RSR4	RSR3	RSR2	RSR1	RSR0	8080h

These *read/write* registers control the output volume of the optional four PCM channels, and values written to the fields behave the same as the Play Master Volume Register (Index 02h), which offers attenuation but no gain. There is an independent mute (1=on) for each channel.

The default value after cold or ~~warm~~ register reset for this register (8080h) corresponds to 0 dB attenuation with mute on.

A.3 "On Demand" Sample Transport Scheme Definitions

AC-link's tag infrastructure imposes FIFO requirements on both sides of the AC-link. For example, in passing a 44.1 kHz stream across the AC-link, for every 480 audio output frames that are sent across, 441 of them must contain valid sample data. Does the AC '97 Digital Controller pass all 441 PCM samples followed by 39 invalid slots? Or does the AC '97 Digital Controller evenly interleave valid and non-valid slots? Each possible method brings with it different FIFO requirements. To achieve interoperability between AC '97 Digital Controllers and Codecs designed by different manufacturers, it is necessary to standardize the scheme for at least one side of the AC-link so that the FIFO requirements will be common to all designs. The Codec side of the AC-link is the focus of this standardization.

The new standard approach calls for the addition of "on demand" slot request flags. These flags are passed from the Codec to the AC '97 Digital Controller during every audio input frame. Each time the AC '97 Digital Controller sees one or more of the newly-defined slot request flags set active (low) in a given audio input frame, it knows that it must pass along the next PCM sample for the corresponding slot(s) in the audio output frame that immediately follows.

A.3.1 Variable Sample Rate Signaling Protocol

For audio, the VRA (Variable Rate Audio) bit in the Extended Audio control register must be set to 1 to enable variable sample rate audio operation. For modem AFE, variable sample rate support is required by definition.

For variable sample rate output, the Codec examines its sample rate control registers, the state of its FIFOs, and the incoming SDATA_OUT tag bits at the beginning of each audio output frame to determine which SLOTREQ bits to set active (low). SLOTREQ bits asserted during the current audio input frame signal which *active output slots* require data from the AC '97 Digital Controller in the next audio output frame. An *active output slot* is defined as any slot supported by the Codec that is not in a power-down state. For fixed 48 kHz operation the SLOTREQ bits are always set active (low) and a sample is transferred in each frame.

For variable sample rate input, the tag bit for each input slot indicates whether valid data is present or not. Thus, even in variable sample rate mode, the Codec is always the master: for SDATA_IN (Codec to Controller), the Codec sets the TAG bit; for SDATA_OUT (Controller to Codec), the Codec sets the SLOTREQ bit and then checks for the TAG bit in the next frame.

Setting the Variable Rate Audio (VRA=1) bit in the Extended Audio Status and Control register has two functions in an AC '97 2.0 Codec:

- Enables PCM DAC and ADC conversions at variable sample rates by write enabling sample rate registers 2C-34h.
- Enables the on demand Codec-to-Controller signaling protocol using SLOTREQ bits that becomes necessary when a DACs sample rate varies from the 48 kHz AC-link serial frame rate

The table below summarizes the behavior:

AC '97 2.0 functionality	**VRA=0**	**VRA=1**
SLOTREQ bits	always 0 (data each frame)	0 or 1 (data on demand)
sample rate registers	forced to 48 kHz	writable

Table 33. VRA Behavior

On reset, the audio sample rate registers default to 48 kHz, and VRA=0. Whenever VRA is set to 0 the registers are forced to BB80h (48 kHz) because that is the only rate supported, and any values previously written to these registers are lost.

VRM=1 controls the optional MIC ADC behavior in the same way that VRA=1 controls the PCM ADC.

Note that modem converters (line1, line2, handset) are not affected by the VRA bit, and SLOTREQ bits for active modem DACs are always treated as valid (data on demand).

For optional Double-Rate Audio operation the *n+1* sample output slots 10-12 must be employed. Setting the Double Rate Audio (DRA=1) bit in the Extended Audio control register indicates that data from PCM L and PCM R in output slots 3 and 4 is to be used in conjunction with PCM L (n+1) and PCM R (n+1) data in output slots 10 and 11, to provide DAC streams at twice the sample rate designated by the PCM front rate control register. Multi-channel Codecs that support PCM Center additionally combine output slots 6 and 12.

It is currently acceptable (from both the technical and market standpoints) to support 96 kHz DVD content via down-sampling to 48 kHz for high quality rendering, therefore Double-Rate Audio is not a recommendation at this time. With regard to double-rates and the independence of front, surround, and LFE channels, it is recommended that audio vendors actively track the status of the various proposals for high quality DVD "pure audio" which are being presented to the RIAA's International Steering Committee (ISC) and DVD Forum working group.

Note that DRA can be used without VRA; in that case the converter rates are forced to 96 kHz if DRA=1.

A.3.2 Input Slot 1: Status Address Port / SLOTREQ Bits

Audio Input Frame Slot #1, the Status Address Port, now delivers Codec control register read address *and* variable sample rate slot request flags for all output slots. Ten of the formerly-reserved least significant bits have been defined as data request flags for output slots 3-12.

Input Slot 1	
Bit	**Description**
19	RESERVED (Set to 0)
18-12	Control Register Index (Set to 0s if tagged "invalid" by AC '97)
11-2	**On Demand Data Request Flags (next output frame):** 0= send data, 1= do NOT send data
11	Slot 3 request: PCM Left channel
10	Slot 4 request: PCM Right channel
9	Slot 5 request: Modem Line 1
8	Slot 6 request: PCM Center
7	Slot 7 request: PCM Left surround
6	Slot 8 request: PCM Right surround
5	Slot 9 request: PCM LFE
4	Slot 10 request: Modem Line 2 or PCM Left (n+1)
3	Slot 11 request: Handset or PCM Right (n+1)
2	Slot 12 request: PCM Center (n+1)
1,0	RESERVED (Set to 0)

Table 34. Input Slot 1-Bit Definitions

The Audio Input Frame Slot 1 tag bit is independent of the bit 11-2 slot request field, and ONLY indicates valid Status Address Port data (Control Register Index). The Codec should only set SDATA_IN tag bits for Slot 1 (Address) and Slot 2 (Data) to 1 when returning valid data from a previous register read. They should otherwise be set to 0. SLOTREQ bits have validity independent of the Slot 1 tag bit.

SLOTREQ bits are always 0 in the following cases

- Non-variable rate Codec
- fixed rate mode (VRA=0)
- inactive (powered down) DAC channel (VRA=0 or 1)

SLOTREQ bits are only set to 1 by the Codec in the following case

- Variable rate audio mode (VRA=1) AND active (power ready) DAC AND a non-48 kHz DAC sample rate and Codec does not need a sample

A.3.3 SLOTREQ Behavior and Power Management

SLOTREQ bits for fixed rate, powered down, and all unsupported Slots should be driven with 0s for maximum compatibility with the original AC '97 Component Specification. When a DAC channel is powered down, it disappears completely from the serial frame: output tag and slot are ignored, and the SLOTREQ bit is absent (forced to zero). The SLOTREQ bit should be forced to 1 in the interval between when the power-down bit for its associated channel is turned off and when its channel is ready to accept samples. Controllers can take advantage of this scheme to eliminate the need to poll the AC '97, AMC '97 or MC '97 status registers.

When the Controller wants to power-down a channel, all it needs to do is:

1. Disable source of DAC samples in Controller
2. Set PR bit for DAC channel in AC97 registers 26h, 2Ah, or 3Eh

When it wants to power up the channel, all it needs to do is:

1. Clear PR bit for DAC channel in AC98 registers 26h, 2Ah, or 3Eh
2. Enable source of DAC samples in Controller

Appendix B. AC '97 2.0 Modem AFE Extension

B.1 Introduction

The purpose of this extension is to define optional interoperable methods for implementing modem analog front-end (AFE) functionality and accessing it via AC-link. This includes:

- Slot assignments for line, handset, and GPIO pin status and control
- Modem AFE register definitions
- GPIO pin status and control definitions
- Power management and wake-up event definitions
- CallerID string transmission via AC-link definitions
- Loopback testing definitions

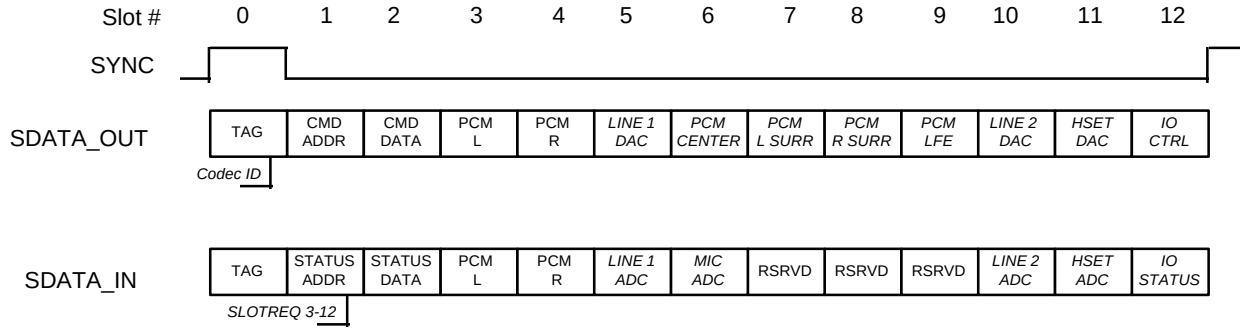


Figure 27. Audio and Modem Slot Assignments

B.2 Slot Assignments for Line, Handset, and GPIO Pin Status and Control

As shown in Figure 27, the line1, line2, and handset streams have been assigned to slots 5, 10, and 11 respectively. As with AC '97, the leading 16-bits of each slot must contain valid sample data; support for 18- or 20-bits is optional. The following table describes the input and output slot data format.

Input and Output Slots 5, 10, 11: Line1, Line2, Handset ADCs and DACs	
Bit	**Description**
19-4	16-bit sample (MSB bit 19, LSB bit 4)
3-0	*Optional: LSBs of 18 or 20-bit sample*

Table 35. Slots 5, 10, and 11-Bit Definitions

Up to 16-bits of GPIO status (input) and control (output) have been directly assigned to bits on slot 12 in order to minimize latency of access to changing conditions. Table 36 describes the GPIO output and input slot assignments.

Input and Output Slot 12: GPIO Pin Status and Control	
Bit	**Description**
19-4	up to 16 GPIO pins (see *GPIO Status and Control Bit Definitions* below)
3-1	Reserved
0	GPIO_INT mask enabled input pin event interrupt (1=event) (input Slot 12 only)

Table 36. Slot 12-Bit Definitions

B.3 Modem AFE Register Definitions

B.3.1 Extended Modem ID Register (Index 3Ch)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
3Ch	Extended Modem ID	ID1	ID0	x	x	x	x	x	x	x	x	x	CID2	CID1	HSET	LIN2	LIN1	xxxxh

The extended modem ID is a *read/write* register that primarily identifies the enhanced Codec's modem AFE capabilities. The default value will depend on features and hardware configuration. Writing any value to this register performs a warm modem AFE reset (register range 3C-56h), including GPIO (register range 4C-54h). The warm reset causes all affected registers to revert to their default values. Note: for AMC '97 parts the audio and modem AFE should be logically independent (writes to register 0h resets audio only).

- LIN1=1 indicates 1st line is supported
- LIN2=1 indicates 2nd line is supported
- HSET=1 indicates handset DAC/ADC is supported
- CID1=1 indicates that caller ID decode for line 1 is supported
- CID2=1 indicates that caller ID decode for line 2 is supported
- ID1, ID0 is a 2-bit field which indicates the Codec configuration: Primary is 00; Secondary is 01, 10, or 11

If LIN1=1, then the Codec is an (A)MC '97, and all modem functionality should be implemented and controlled via the newly-defined Extended AC '97 registers. In particular, it is required that the following functionality NOT be implemented as defined in the original AC 97 Component Specification:

- Reset Register (Index 0h) bit 1: Modem line Codec support (ID1)
- Reset Register (Index 0h) bit 6-9 audio DAC and ADC resolution do not have any MAFE resolution information
- General Purpose Register (Index 20h) bits 10, 11: Local Loop Back (LLBK) and Remote Loop Back (RLBK)
- Modem Rate (Index 24h) Register
- Power-down/Ctrl/Stat (Index 26h) bits 4 ,15: Modem Ready (MDM) and Modem DAC/ADC off (PR7)

The value after cold or ~~warm~~ register reset for this register is constant, and depends on features supported and hardware configuration as Primary or Secondary Codec.

B.3.2 Extended Modem Status and Control Register (Index 3Eh)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
3Eh	Ext'd Modem Stat/Ctrl	PRH	PRG	PRF	PRE	PRD	PRC	PRB	PRA	HDAC	HADC	DAC2	ADC2	DAC1	ADC1	MREF	GPIO	FFxxh

The Extended Modem Status and Control register functions similarly to the original AC '97 Power-down Control/Status register, located at index 26h. The (A)MC '97 Codec must restrict modem and handset power-down control/status to this register since all of the functions are provided here. Therefore, the (A)MC '97 Codec (and AC '97 Digital Controller, of course) must ignore bits MDM and PR7 in register 26h and use what is included here. When the GPIO section is powered down, all outputs must be tri-stated and input slot 12 should be marked invalid when the AC-link is active. When slot 12 is invalid, register 54h (GPIO Pin Status Register) will report 0s. In addition the Codec should force SDATA_IN slot 12 to all 0s.

Bits 7-0 are *read only*, 1 indicates modem AFE subsystem readiness:

- GPIO=1 indicates GPIO ready
- MREF=1 indicates Modem Vref's up to nominal level
- ADC1=1 indicates Modem Line 1 ADC ready
- DAC1=1 indicates Modem Line 1 DAC ready
- ADC2=1 indicates Modem Line 2 ADC ready
- DAC2=1 indicates Modem Line 2 DAC ready
- HADC=1 indicates Handset ADC ready

- HDAC=1 indicates Handset DAC ready

Bits 15-8 are *read/write* and control modem AFE subsystem power-down. For AMC '97 implementations which use a common AREF and MREF, both power-down bits must be low for disabling the reference.

- PRA=1 indicates GPIO power-down
- PRB=1 indicates Modem Vref off
- PRC=1 indicates Modem Line 1 ADC off
- PRD=1 indicates Modem Line 1 DAC off
- PRE=1 indicates Modem Line 2 ADC off
- PRF=1 indicates Modem Line 2 DAC off
- PRG=1 indicates Handset ADC off
- PRH=1 indicates Handset DAC off

Bits 7-0 are *read only*, 1 indicates modem AFE subsystem readiness. Bits 15-8 are *read/write* and control modem AFE subsystem power-down. For AMC '97 implementations which use a common AREF and MREF, both power-down bits must be low for disabling the reference.

The default value after cold or ~~warm~~ register reset for this register (FFxxh) is all extended features powered down (D15-D8=1). The feature readiness status should always be accurate (D7-D0=x).

B.3.3 Modem Sample Rate Control Registers (Index 40h – 44h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
40h	Line1 DAC/ADC Rate (input, output slot 5)	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
42h	Line2 DAC/ADC Rate (input, output slot 10)	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
44h	Handset DAC/ADC Rate (input, output slot 11)	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

For modem AFE, each DAC/ADC pair is governed by a read/write modem sample rate control register that contains a 16-bit unsigned value between 0 and 65535, representing the rate of operation in Hz. Any number written over BB80h will cause the sample rate to be 48 kHz. For all rates, if the value written to the register is supported that value will be echoed back when read, otherwise the closest (higher in case of a tie) rate supported is returned.

For all modem AFE implementations, Table 37 defines the minimum set of sample rates that must be supported in **bold** typeface; other recommended rates are shown in *italics*. Although bit fields could be used to support the relatively few required and recommended sample rates, a full 16-bit register was chosen as the most flexible way to support future expandability.

Support for the one required and two optional non-integer sample rates, 13,714.28 (96000/7), 8228.57 (57600/7), and 10285.71 (72000/7), requires that the Codec automatically recognize the non-integer rate from the integer portion.

Variable sample rate operation for modem AFE, utilizing SLOTREQ signaling as defined in AC '97 2.0 Appendix A is a requirement for AC '97 2.1 compliance.

Required (√) and *recommended (+)* sample rates for modem AFE (Hz)			
Sample rate	**D15-D0**	**line1, line2**	**handset**
7200	*1C20*	+	
8000	**1F40**	√	√
8228.57 (57600/7)	*2024*	+	
8400	*20D0*	+	
9000	*2328*	+	
9600	**2580**	√	
10285.71 (72000/7)	*282D*	+	
12000	*2EE0*	+	
13,714.28 (96000/7)	**3592**	√	
16000	**3E80**	√	√
19200	*4B00*	+	
24000	5DC0		
48000	BB80		

Table 37. Sample Rates for Modem AFE (Hz)

Note: To comply with ITU-T modem recommendations, sample rates must be generated to a tolerance of +/- 0.01%. This includes crystal tolerance, including variations over voltage, temperature, and age.

The default value after cold or ~~warm~~ register reset for these registers (BB80h) is 48 kHz.

B.3.4 Modem DAC/ADC Level Control Registers (Index 46h – 4Ah)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
46h	Line 1 DAC/ADC level	mute	x	x	x	DAC3	DAC2	DAC1	DAC0	mute	x	x	x	ADC3	ADC2	ADC1	ADC0	8080h
48h	Line 2 DAC/ADC level	mute	x	x	x	DAC3	DAC2	DAC1	DAC0	mute	x	x	x	ADC3	ADC2	ADC1	ADC0	8080h
4Ah	Handset DAC/ADC level	mute	x	x	x	DAC3	DAC2	DAC1	DAC0	mute	x	x	x	ADC3	ADC2	ADC1	ADC0	8080h

These *read/write* registers control the modem AFE DAC and ADC levels. DAC levels are defined to be the same as AC '97 Play Master Volume Register (2-6h minus 5th and 6th bits); ADC levels are defined to be the same as AC '97 Record Gain Registers (1C-1Eh).

The default value after cold or ~~warm~~ register reset for these registers (8080h) corresponds to 0 dB DAC attenuation with mute on, 0 dB ADC gain/attenuation with mute on.

B.3.5 GPIO Pin Configuration Register (Index 4Ch)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
4Ch	GPIO Pin Config (0 =output, 1=input)	GC15	GC14	GC13	GC12	GC11	GC10	GC9	GC8	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	FFFFh

The GPIO Pin Configuration is a read/write register that specifies whether a GPIO pin is configured for input (1) or for output (0), and is accessed via the standard slot 1 and 2 command address/data protocols.

If a GPIO pin is implemented, the respective GCx bit should be read/writable and set to 1. If a GPIO is not implemented, then the respective GCx bit should be read-only and set to 0. This informs the software how many GPIO pins have been implemented. It is up to the AC '97 Digital Controller to send the desired GPIO pin value over output slot 12 in the outgoing stream of the AC-link before configuring any of these bits for output.

The default value after cold or ~~warm~~ register reset for this register (FFFFh), is all pins configured as inputs.

B.3.6 GPIO Pin Polarity/Type Register (Index 4Eh)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
4Eh	GPIO Pin Polarity/Type (0 =low, 1=high active)	GP15	GP14	GP13	GP12	GP11	GP10	GP9	GP8	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	FFFFh

The GPIO Pin Polarity/Type is a read/write register that defines GPIO Input Polarity (0=Low, 1=High active) when a GPIO pin is configured as an Input. It defines GPIO Output Type (0=CMOS, 1=OPEN-DRAIN) when a GPIO pin is configured as an Output.

The default value after cold or ~~warm~~ register reset for this register (FFFFh) is all pins active high. Non-implemented GPIO pins always return 1s.

B.3.7 GPIO Pin Sticky Register (Index 50h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
50h	GPIO Pin Sticky (0 =not sticky, 1=sticky)	GS15	GS14	GS13	GS12	GS11	GS10	GS9	GS8	GS7	GS6	GS5	GS4	GS3	GS2	GS1	GS0	0000h

The GPIO Pin Sticky is a read/write register that defines GPIO Input Type (0=Non-Sticky, 1=Sticky) when a GPIO pin is configured as an input. GPIO inputs configured as Sticky are cleared by writing a 0 to the corresponding bit of the GPIO Pin Status register 54h (see below), and by reset.

The default value after cold or ~~warm~~ register reset for this register (0000h) is all pins non-Sticky. Unimplemented GPIO pins always return 0s. Sticky is defined as Edge sensitive, Non-Sticky as Level-sensitive.

B.3.8 GPIO Pin Wake-up Mask Register (Index 52h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
52h	GPIO Pin Wake-up (0 =no int, 1=yes int)	GW15	GW14	GW13	GW12	GW11	GW10	GW9	GW8	GW7	GW6	GW5	GW4	GW3	GW2	GW1	GW0	0000h

The GPIO Pin Wake-up is a read/write register that provides a mask for determining if an input GPIO change will generate a wake-up or GPIO_INT (0=No, 1=Yes). When the AC-Link is powered down (Register 26h PR4 = 1 for Primary Codecs), a wake-up event will trigger the assertion of SDATA_IN (the AC-Link wake-up protocol is defined in Appendix C). When AC-link is powered up, a wake-up event will appear as GPIO_INT=1 on bit 0 of input slot 12.

An AC-Link wake-up Interrupt is defined as a 0 to 1 transition on SDATA_IN when the AC-Link is Powered down (Register 26h PR4=1). GPIO bits that have been programmed as Inputs, Sticky and Pin Wake-up, upon transition either (high-to-low) or (low-to-high) depending on pin polarity, will cause an AC-Link wake-up event (transition of SDATA_IN from 0 to 1), if and only if the AC-Link was powered down.

The default value after cold or ~~warm~~ register reset for this register (0000h) defaults to all 0s specifying no wake-up event. Non-implemented GPIO pins always returns 0s.

B.3.9 GPIO Pin Status Register (Index 54h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
54h	GPIO Pin Status (slot 12, bits 15-0)	GI15	GI14	GI13	GI12	GI11	GI10	GI9	GI8	GI7	GI6	GI5	GI4	GI3	GI2	GI1	GI0	xxxxh

The GPIO Status is a read/write register that reflects the state of all GPIO pins (inputs and outputs) on slot 12. The value of all GPIO pin inputs and outputs comes in from the Codec every frame on slot 12, but is also available for

reading as GPIO Pin Status via the standard slot 1 and 2 command address/data protocols. GPIO inputs configured as Sticky are cleared by writing a 0 to the corresponding bit of this register 54h.

Bits corresponding to unimplemented GPIO pins should be forced to zero in this register and input slot 12.

GPIO bits that have been programmed as Inputs and Sticky, upon transition either (high-to-low) or (low-to-high) depending on Pin polarity, will cause the individual GI bit to go asserted 1, and remain asserted until a write of 0 to that bit. The only way to set the desired value of a GPIO output pin is to set the control bit in output slot 12.

The default value, if configured as an input, after cold or ~~warm~~ register reset for this register is always the state of the GPIO pin.

B.3.10 Miscellaneous Modem AFE Status and Control Register (Index 56h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
56h	Miscellaneous Modem AFE Stat/Ctrl	CID2	CID1	CIDR	MLNK	x	HSB2	HSB1	HSB0	x	L2B2	L2B1	L2B0	x	L1B2	L1B1	L1B0	x000h

This *read/write* register defines the loop back modes available for the modem line and handset ADCs/DACs described in section B.6. It also supports the optional CID bits described in section B.5.4.

- L1B2-0 controls Line 1 loopback modes (or disabled)
- L2B2-0 controls Line 2 loopback modes (or disabled)
- HSB2-0 controls Handset loopback modes (or disabled)
- MLNK controls a MC '97s AC-link status. 1 sets the MC '97s AC-link to off (sleep), 0 sets the link on (active).
- CID1=1 indicates caller ID decode for Line 1 is supported
- CID2=1 indicates caller ID decode for Line 2 is supported
- CIDR=1 indicates that called ID data is "raw" (demodulated but not decoded; includes seizure, marks, etc.)

The default value after cold or ~~warm~~ register reset for this register (x000h) is all loopbacks disabled, and dependent on the caller ID features.

B.4 GPIO Pin Definitions

GPIO pins are programmable to have input/output functionality. The data values (status) for these pins are all in one register with input/output configuration in a separate register. Control of GPIO pins configured for output is achieved by setting the corresponding bit in output slot 12; status of GPIO pins configured for input is returned on input slot 12.

The Codec must constantly set the GPIO pins that are configured for output, based upon the value of the corresponding bit position of the control slot 12. The Codec should ignore output slot 12 bits that correspond to GPIO control pins configured as inputs. The Codec must constantly update status on input slot 12, based upon the logic level detected at each GPIO pin configured for input. A GPIO output pin value that is written via slot 12 in the current frame won't affect the GPIO status that is returned in that particular write frame.

This slot 12-based control/status protocol minimizes the latency and complexity, especially for host-based Controllers and host data pump software, and provides high speed monitoring and control, above what could be achieved with command/status slots. For host-based implementations most AC '97 registers can be shadowed by the driver in order to provide immediate response when read by the CPU, and GPIO pins configured as inputs should be capable of triggering an interrupt upon a change of status.

The AC-link request for GPIO pin status is always delayed by at least one frame time. Read-Modify-Writes across the AC-link will thus incur latency issues and must be accounted for by the software driver or AC '97 Digital Controller firmware. PCI retries must be kept to a minimum wherever possible.

B.4.1 GPIO Pin Implementation

The modem AFE contains a number of General Purpose Input/Outputs suitable for easy connection with minimal parts to a DAA circuit. There is no requirement that a GPIO, when configured as output, must be able to directly drive a relay coil. The AC '97 Digital Controller is responsible for configuring any GPIOs as outputs on power-up, in order to drive transistors appropriately for DAA control.

When configured as an input, a GPIO must function as a CMOS Schmitt-triggered input for a 3.3V power supply. to To conserve power internal pull-ups or pull-downs should not be present. The board designers are responsible for connecting unused pins to DVdd or DVss.

The GPIOs must be tri-stated to a high impedance state on power-on or a cold reset. It is up to the AC '97 Digital Controller to first enable the output after setting it to the desired state. To prevent overdrive of any transistors, the outputs should have slow rise and fall times. Typical values should be 40 nsec for 10% to 90% of DVdd with a 50 pF load. In addition, the device must sink 2-4 mA at a maximum level of 0.4V and must source 2-4 mA at a minimum level of 2.4V.

The previous rise/fall, and source/sink are provided as implementation examples, and are not requirements for AC '97 2.1 compliance.

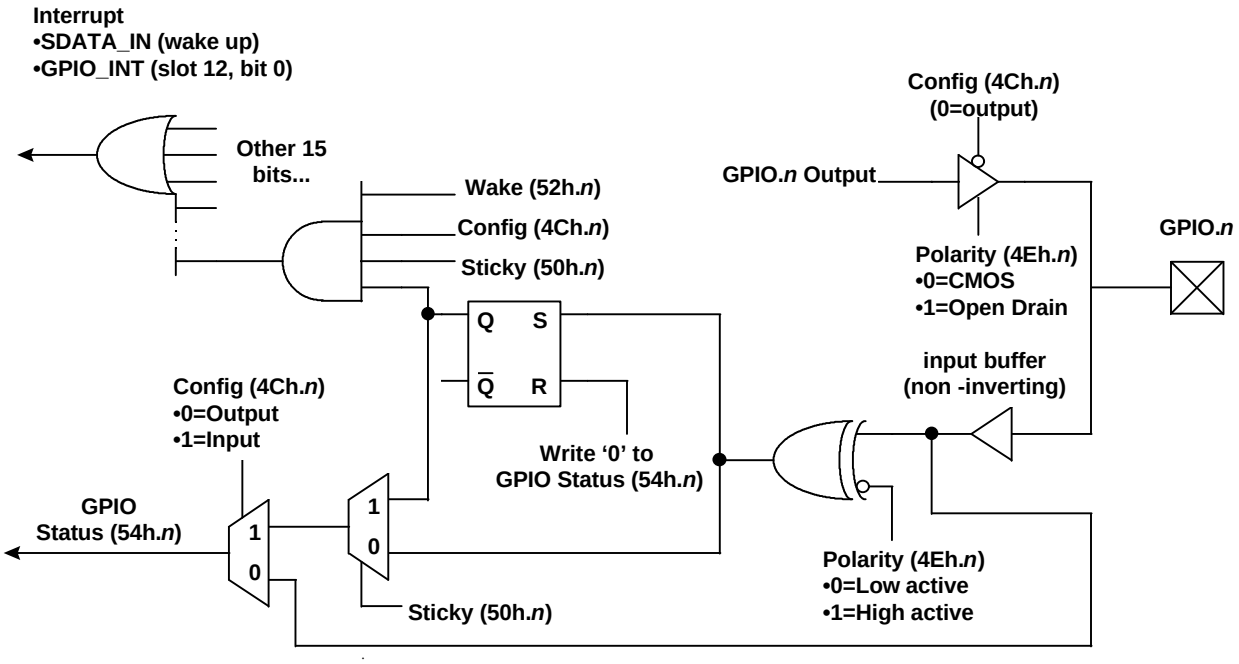


Figure 28. "Conceptual" Example of GPIO Pin Implementation

B.4.2 Recommended Slot 12 GPIO Bit Definitions

Slot 12 (Input and Output): GPIO bits				
Bit	**GPIO**	**Name**	**sense**	**Description**
19	GPIO15	LINE2_HL2R	out	opt GPIO / HANDSET_TO_LINE2 relay control (out)
18	GPIO14	LINE2_PULSE	in/out	opt GPIO / Line 2 pulse dial (out)
17	GPIO13	LINE2_LCS	in	Loop Current Sense Line 2
16	GPIO12	LINE2_CID	out	Caller ID path enable Line 2
15	GPIO11	LINE2_RI	in	Ring Detect Line 2
14	GPIO10	LINE2_OH	out	Off Hook Line 2
13	GPIO9	LINE12_RS	in/out	opt GPIO / International Bit 3 / Line 1/2 RS (out)
12	GPIO8	LINE12_DC	in/out	opt GPIO / International Bit 2 / Line 1/2 DC (out)
11	GPIO7	LINE12_AC	in/out	opt GPIO / International Bit 1 / Line 1/2 AC (out)
10	GPIO6	LINE1_HOHD	in/out	opt GPIO / HANDSET off hook detect (in)
9	GPIO5	LINE1_HL1R	in/out	opt GPIO / HANDSET to Line 1 relay control (out)
8	GPIO4	LINE1_PULSE	in/out	opt GPIO / Line 1 pulse dial (out)
7	GPIO3	LINE1_LCS	in	Loop Current Sense Line 1
6	GPIO2	LINE1_CID	out	Caller ID path enable Line 1
5	GPIO1	LINE1_RI	in	Ring Detect Line 1
4	GPIO0	LINE1_OH	out	Off Hook Line 1
1-3		Vendor rsrvd		vendor optional
0		GPIO_INT		GPIO_INT (uses same logic as wake-up event)

Table 38. Recommended Slot 12 GPIO Bit Definitions

AC '97 2.0 makes no requirement on the number of GPIOs or their use, only that they be implemented as general purpose. Recommended bit definitions are provided for maximum interoperability, and should be followed wherever possible.

The suggested use for the International Bits 1-3 is to implement LINE12_AC, LINE12_DC, and LINE12_RS, which, when set to one, adjust the DAA AC impedance, DC impedance, and Ring Detect sensitivity to alternate values more suitable for some non-North American countries. These outputs have effect on both Line 1 and Line 2 (that is, it is assumed that both DAAs reside in the same country).

Outputs LINE1_PULSE and LINE2_PULSE control pulse dial relays, separate from the Off Hook relays, used in DAAs for some non-North American DAAs.

GPIO_INT has been added to leverage the logic that has already been implemented within the Codec to detect a change in GPIO input state and trigger a wake-up event. When the Codec is NOT in power-down mode any input GPIO change can be enabled by the wake-up mask to generate GPIO_INT=1, to indicate to the controller or driver that the GPIO state has changed and should be updated in memory. The controller acknowledges and clears a wake-up event or GPIO_INT by writing a 0 to the corresponding bit in register 54h. This supports shadowing of Codec registers in memory by potentially eliminating polling.

B.5 Wake up and Power Management Event (PME#) Support

Ring and handset offhook detect are examples of events that might need to wake-up a PC that has suspended into a low power state. Wake up on an audio event could eventually become practical.

Revision 1.x AC '97 architecture enables fine granular power management of the AC-link and the individual subfunctions within the Codec. However it does not support system wake requests triggered by external events. Power management, or wake, event support for a modem is a key feature of Intel's Instantly Available PC architecture and must be fully-comprehended by the Extended AC '97 architecture. Support for wake-up must be

comprehended for various configurations of AC ’97 and (A)MC ’97, be they single Codec, or split partitioned primary/secondary Codec implementations.

Instantly Available PC architecture specifies a Vaux supply that is designed to support specific “always active” functions while the majority of the PC is powered down. 5.0 V *and* 3.3 V Vaux supplies are available on the motherboard, and a 3.3 V Vaux supply pin is currently being added to the PCI slot definition. The cleanliness of the Vaux supply will depend on the power supply source.

B.5.1 Combined Audio/Modem AFE Codec (AMC ’97)

For additional discussions of AMC and AC + MC power management see AC ’97 2.1 Appendix D section D.4.

For AMC ’97 combined Audio/Modem AFE implementations the Codec, AC-link and portions of the AC ’97 Digital Controller ***which provide wake-up functionality***, all must be powered by Vaux as illustrated in Figure 29:

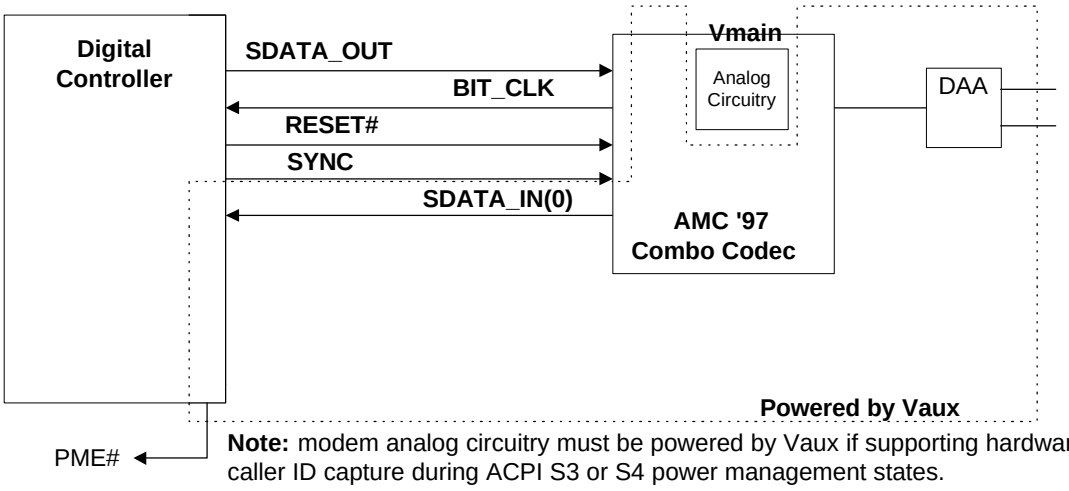


Figure 29. Combined Audio / Modem AFE Auxiliary Power Distribution

The Codec and AC-link are programmed to a low power state (see Figure 30) and, upon detection of a power management event, are brought back to the active state by executing a warm reset sequence as shown in Figure 31.

Figure 30 shows the AC ’97 Digital Controller placing the AC-link into its lowest power state by programming the Codec’s Power-down Control/Status register with bit(12) = 1 (PR4) .

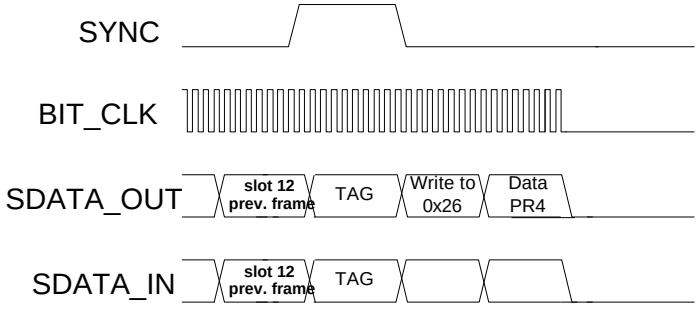


Figure 30. AC-link Low Power Mode

In response to this command BIT_CLK and SDATA_IN Codec, and SDATA_OUT controller outputs go low and

stay low.

AC-link when programmed to its low power mode, can be reactivated only by the device driver, which can write to a AC ’97 Digital Controller register causing it to signal a cold or warm reset on the AC-link. A warm reset, which will not alter the current AC ’97 registers, is signaled by driving SYNC high for a minimum of 1us in the absence of BIT_CLK.

Within normal audio frames SYNC is a synchronous Codec input. However, in the absence of BIT_CLK, SYNC is treated as an asynchronous input used to signal a warm reset to the AC ’97 Codec.

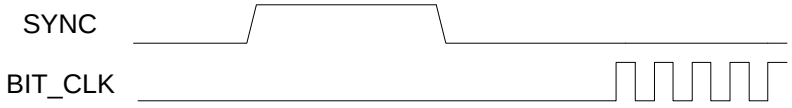


Figure 31. AC-link Warm Reset

In an AMC ’97 implementation, where the audio/modem AFE Codec and AC-link are both completely powered by Vaux, an enabled power management event detected at the modem interface causes the assertion of the PME# signal to the system. PME# assertion causes the system to resume so that the modem event can be serviced. The first thing that the device driver must do to reestablish communications with the Codec is to command the AC ’97 Digital Controller to execute a warm reset to the AC-link. Figure 32 illustrates the entire sequence:

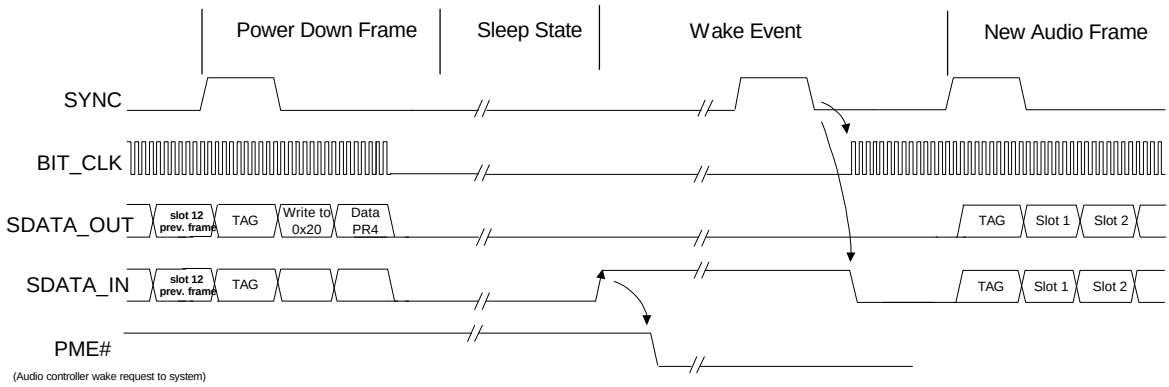


Figure 32. AC-link Power-down/Up Sequence

The rising edge of SDATA_IN causes the AC ’97 Digital Controller to assert its PME# to the system’s ACPI controller. The AMC ’97 Codec must keep SDATA_IN high until it has sampled SYNC having gone high, and then low. PME# is cleared out in the AC ’97 Digital Controller by system software, asynchronous to AC-link activity. The AC ’97 Digital Controller must always monitor the Codec’s ready bit before sending data to it.

B.5.2 Split Partitioned Implementations (AC ’97 2.0 + MC ’97)

For additional discussions of AMC and AC + MC power management see AC ’97 2.1 Appendix D section D.4.

In a split partitioned implementation, where separate audio and modem AFE Codecs are employed, the MC ’97 Codec, its DAA, a common clock oscillator, and portions of the AC ’97 Digital Controller are powered by Vaux. The AC ’97 audio-only Codec is powered via its normal DVdd, and AVdd supplies, and as such is shut completely off when the system enters a sleeping state. Figure 33 shows an example of a split partitioned Codec implementation.

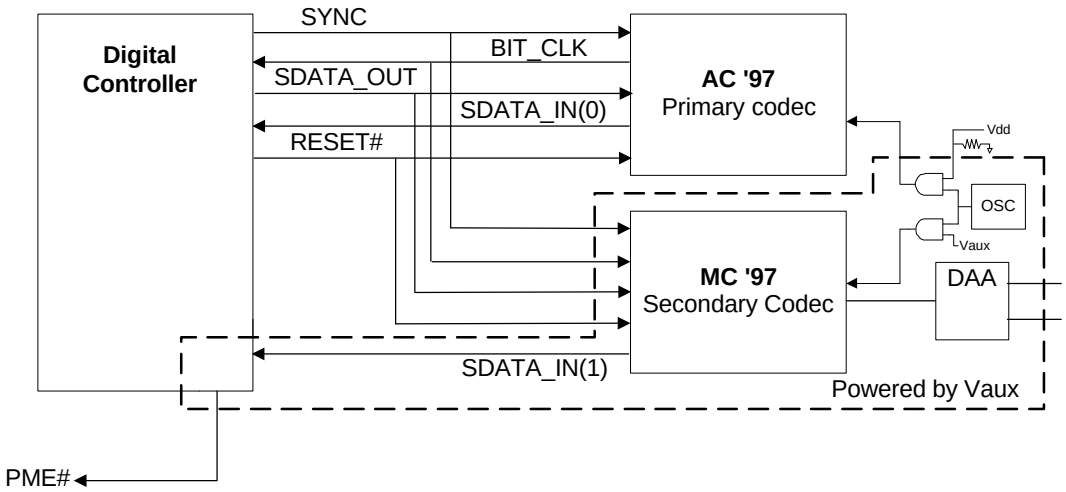


Figure 33. Split Partitioned Design Example

Once the system enters a sleeping state Vdd shuts off, which causes the oscillator input to the AC '97 to go low and remain low. Clocking remains active at the MC '97, which continues to look for ring detection and Caller ID data while the rest of the system sleeps. A wake or power management event causes the MC '97 to transition its SDATA_IN from low to high, which in turns causes the AC '97 Digital Controller to assert PME# to the system. Once the main power has been reapplied the device driver executes a cold or warm AC-link reset followed by the restoration of any saved off functional context. Following SDATA_IN's low-to-high transition as a result of a Power Management event, it must remain high until either a warm or cold reset is observed on the AC-Link.

B.5.2.1 The MLNK bit

For additional discussion of AMC or AC + MC power management see AC '97 2.1 Appendix D section D.4.

B.5.3 Wake Up and Voltage Sequencing

For additional discussion of AMC or AC + MC power management see AC '97 2.1 Appendix D section D.4.

AC '97 Codecs have both analog and digital supply pins defined. There are no voltage sequencing requirements for AVdd and DVdd specifying which voltage source ramps up or down first.

In an Instantly Available PC the main Vdd voltage rails will be shut off under program control in order to achieve a very low power, yet connected, state. Auxiliary power (Vaux), will remain active in the system to keep portions of the modem alive[12]. Codec designs that support separate voltage inputs for analog and digital sections must comprehend this so that no device damage or malfunction can occur as a result of the main voltage dropping off while the auxiliary supply remains active.

B.5.4 Wake Up and Caller ID Decode in the Controller and/or Codec

For additional discussion of AMC or AC + MC power management see AC '97 2.1 Appendix D section D.4.

The resume time for a PC in D3 low power state makes it unlikely that a driver will completely load in time to wake-up the AC '97 Digital Controller and enable it to capture Caller ID data on the line. Therefore either the AC '97 Digital Controller or (A)MC '97 Codec must be able to store this information while the driver continues to initialize. In the case of the combined Codec (AMC '97), the entire Codec, AC-link, and portions of the AC '97 Digital Controller are powered by Vaux which enables Caller ID decode and store to be done either by the controller or by the modem AFE Codec. However in the case of the split partitioned design, only the MC '97 SDATA_IN

[12] This includes all logic required to detect the external wake event, and then to report it across the AC-link.

signal on the AC-link is powered while the remainder of the AC-link is un-powered. In this case the Caller ID decode and store operations must be supported in the MC '97 Codec.

If the maximum delay from a PME# event to power pins on the PCI Bus at 95% full value is under 2 seconds, controller manufacturers may be able to load the Caller ID code and wait for the incoming data before the driver has had an opportunity to configure the part and assign it resources. The controller then may present the Caller ID data to the driver when it is loaded.

The resume time for a PC in D3 cold also precludes *host-based processing of the caller ID burst*, in both the U.S. and Europe. (A)MC '97 Codecs which serve as the AFE for host-based modem implementations may find it attractive to support Caller ID decode functionality in addition to simple wake-up on ring detect. Such a Codec would be able to automatically decode and save the caller ID string until the PC system and AC '97 Digital Controller have resumed.

The optional CID1 and CID2 bits in the Miscellaneous Modem AFE Status and Control register have been defined to indicate to the awakened AC '97 Digital Controller that decoded caller ID string data is available for Line1 (CID1=1) or Line2 (CID2=1). ADC input slots 5 (for Line 1) and 10 (for Line 2) can be used to transfer the caller ID string data, two bytes per audio input frame until completed, at which time the CIDn bit automatically resets (goes inactive).

The AC '97 Digital Controller initiates the caller ID string transfer by strobing (writing) CIDn=1 and subsequently reading data from input slot 5 (for Line 1) or 10 (for Line 2) until the tag bits and the CIDn both become inactive. A strobe (write) of CIDn=0 will clear or cancel the caller ID transmission and reset the CIDn indicator. Once the CIDn bit is reset (automatically or manually), the slot resumes transfer of ADC input data.

Data from the caller ID string can be handled two ways. It can either be demodulated only (raw) or demodulated and preprocessed to delete the channel seizure time and mark signal time, etc. It requires slightly more RAM (approx. 50 bytes) to retain a raw string, but less decoder intelligence. The CIDR bit in the Miscellaneous Modem AFE Status and Control register indicates which method the Codec caller ID supports. CIDR=1 indicates that stored caller ID data is raw.

B.6 Loopback Modes for testing

In Local Analog Loopback mode, the analog output from DAC is connected to the analog input of the associated ADC. The DAC output pin(s) are muted and the ADC input pin(s) are ignored. In Remote Analog Loopback mode, The ADC input pin(s) are connected to the DAC pin(s) in addition to the ADC input. The DAC output is ignored.

Bit	Name	Function
2-0	L1B2-L1B0	Modem Line 1 Loop back enable 000 = Disabled (default) 001 = ADC Loop back 010 = Local Analog Loop back 011 = DAC Loop back 100 = Remote Analog Loop back 101 -111 = Vendor optional
6-4	L2B2-L2B0	Modem Line 2 Loop back enable 000 = Disabled (default) 001 = ADC Loop back 010 = Local Analog Loop back 011 = DAC Loop back 100 = Remote Analog Loop back 101-111 = Vendor optional
10-8	HSB2-HSB0	Handset Loop back enable 000 = Disabled (default) 001 = ADC Loop back 010 = Local Analog Loop back 011 = DAC Loop back 100 = Remote Analog Loop back 101-111 = Vendor optional

Table 39. Modem Loopback Control Bit Definitions

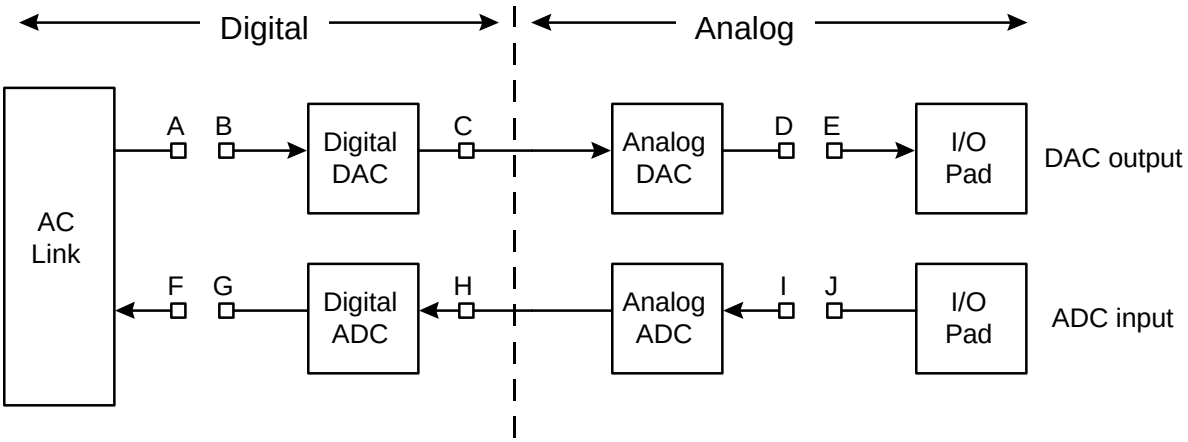


Figure 34. Loopback points

ADC LOOP BACK '001'
The ADC loop back takes the line input signal to the ADC and routes it back to the Line output. This loop includes the analog functions in the receive and transmit path. The path is from the ADC input all the way to point G where it is feed back to point B and out to the DAC output.

LOCAL ANALOG LOOP BACK '010'
The appropriate outgoing slot of the AC-link is passed through the DAC and the analog filters, looped back through the ADC, then onto the appropriate incoming stream slot of the AC-link. This is commonly used in modem modes to troubleshoot problems. This path is from the link (point A) to point D where it is feedback to point I and back through the ADC to the link.

DAC LOOP BACK '011'
This digital test loops back the digital transmit path (outgoing stream) to the digital receive path (incoming stream). This path is from the link (point A) to through the Digital portion of the DAC to point C where it is feedback to point H and back through the digital section of the ADC.

REMOTE ANALOG LOOP BACK '100'
The Line input signal is routed back to the Line output. This loop includes the analog receive functions, but no ADC or DAC. This path is from the ADC input to point J where it is feedback to point E and out to the DAC output.

Appendix C. AC ‘9 2.0 Multiple Codec Extension

C.1 Introduction

Several ways of supporting multiple Codec configurations on AC-link have been implemented or proposed, including Codecs with selective AC-link pass-through and controllers with duplicate AC-links. Multiple Codec implementations that appear as one AC-link device to the Digital Controller remain viable as interoperable solutions.

The purpose of this extension is to define the basic support for alternate partitionings that physically separate AC-link functionality into two or more Codecs, but use a common Digital Controller. Potential implementations include separate Codecs for independent audio and modem AFE functionality and docking stations, where one Codec is in the laptop and another is in the dock.

Table 40 provides several examples of potential two Codec partitionings.

Configuration	Primary / Secondary	Notes
1	AC ’97 1.0 or 2.0 / MC ’97	Separate audio and modem Codecs for desktop
2	AC ’97 1.0 or 2.0 / AC ’97 2.0	Audio only docking
3	AMC ’97 / AMC ’97	Combo docking
4	AMC ’97 / AC ’97 2.0	Combo to audio only docking

Table 40. Potential Two Codec Configurations

This Appendix covers these topics

- Primary and Secondary Codec Definitions
- Secondary Codec Register Access Definitions
- Clocking for Multiple Codec implementations

Please note that the basic support defined in this Appendix may not provide comprehensive solutions for all clocking, power management, hot docking, and docking reset issues.

C.2 Primary and Secondary Codec Definitions

Utilizing the methods defined in this Appendix, there can be up to four Codecs on the extended AC-link. Multiple Codec AC-link implementations must run off a common BIT_CLK. They can potentially save controller pins by sharing SYNC, SDATA_OUT, and RESET# from the AC ’97 Digital Controller. Each device requires its own SDATA_IN pin back to the controller. This prevents contention of multiple devices on one input. It also removes any unnecessary complexity from the Codecs. See Figure 35 for an example of a block diagram.

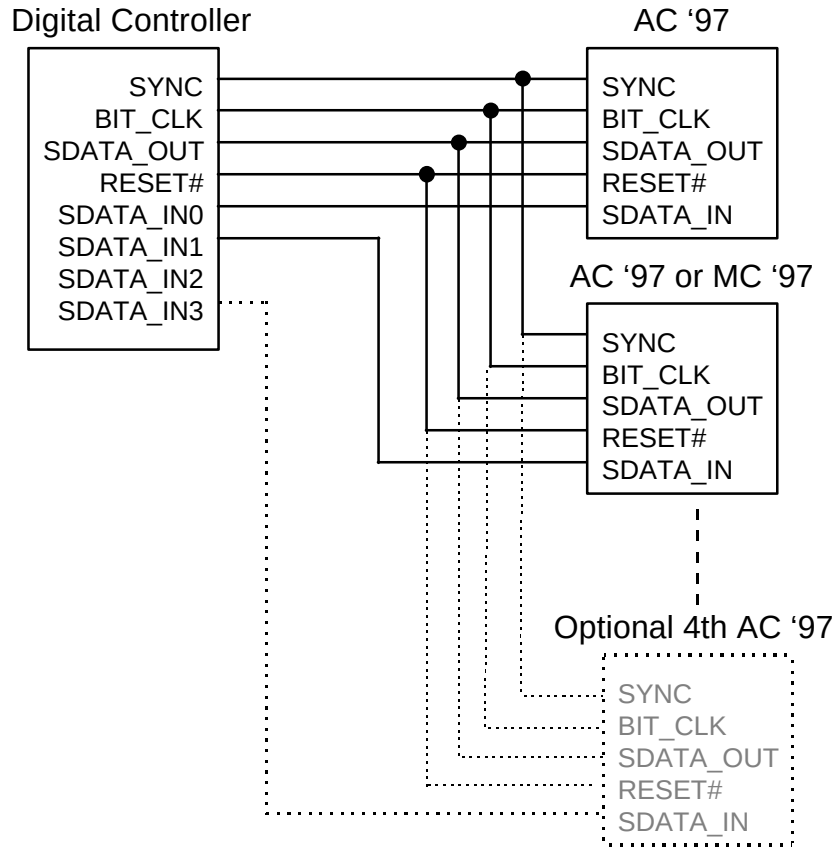


Figure 35. Multiple Codec Example

By definition there can be one Primary Codec (ID 00, includes all AC ’97s) and up to three Secondary Codecs (IDs 01,10, and 11). The Codec ID functions as a chip select. Secondary devices therefore have completely orthogonal register sets; each is individually accessible and they do not share registers

C.2.1 Primary Codec Definitions

The Primary device is completely compatible with existing AC ’97 definitions and extensions. Primary Codec registers are accessed exactly as defined in the AC ’97 Component Specification and AC ’97 Extensions. All AC ’97 devices operate as Primary by definition. Primary AC ’97 2.0 devices must be configurable (via hardwiring, strap pin(s), or other methods) as Codec ID 00 in the two-bit field(s) of the Extended Audio and/or Extended Modem ID Register(s).

A AC ’97 Digital Controller which supports multiple Codec partitioning would implement multiple SDATA_IN inputs to support one primary (AC ’97, AC ’97 2.0 or AMC ’97) Codec and up to three secondary (AC ’97 2.0, AMC ’97, or MC ’97) Codecs.

The Primary Codec generates the master AC-link BIT_CLK for both the AC ’97 Digital Controller and any Secondary Codecs. It is recommended that all AC ’97 Codecs be designed to support at least two (optionally up to

four) 10K Ohm 50 pF loads on the BIT_CLK. This insures that dual (or up to four) Codec implementations will not load down the clock output.

C.2.2 Secondary Codec Definitions

The Secondary device can be only an AC '97 2.0, MC '97, AMC '97 or completely compatible to one of those devices. A secondary device's BIT_CLK pin needs to be configured as an input. Using the BIT_CLK provided by the Primary Codec is necessary to insure that everything on the AC-link will be synchronous. BIT_CLK could also potentially be used as the clock source (multiplied by 2 so that the internal rate is 24.576 MHz).

Secondary devices must be configurable (via hardwiring, strap pin(s), or other methods) as Codec ID 01, 10, or 11 in the two-bit field(s) of the Extended Audio and/or Extended Modem ID Register(s). Secondary Codecs should power up with BIT_CLK configured as an input.

C.3 Secondary Codec Register Access Definitions

In order for the AC '97 Digital Controller to independently access Primary and Secondary Codec registers a 2-bit Codec ID field (chip select) has been added to the previously unused LSBs of Output Slot 0.

Primary Codec access is exactly as defined for AC '97. For Secondary Codec access, the AC '97 Digital Controller must *invalidate* the tag bits for Slot 1 and 2 Command Address and Data (Slot 0, bits 14 and 13) and place a *non-zero* value (01, 10, or 11) into the Codec ID field (Slot 0, bits 1 and 0).

Secondary Codecs disregard the Command Address and Command Data (Slot 0, bits 14 and 13) tag bits when they see a 2-bit Codec ID value (Slot 0, bits 1 and 0) that matches their configuration. In a sense the Secondary Codec ID field functions as an alternative Valid Command Address (for Secondary reads and writes) and Command Data (for Secondary writes) tag indicator.

Secondary Codecs must monitor the Frame Valid bit, and ignore the frame (regardless of the state of the Secondary Codec ID bits) if it is not valid. AC '97 Digital Controllers should set the frame valid bit for a frame with a secondary register access, even if no other bits in the output tag slot except the Secondary Codec ID bits are set.

This method is designed to be backwards-compatible with existing AC '97 controllers and Codecs. There is no change to output Slot 1 or 2 definitions.

Output Tag Slot (16-bits)	
Bit	**Description**
15	Frame Valid
14	Slot 1 Valid Command Address bit (†Primary Codec only)
13	Slot 2 Valid Command Data bit (†Primary Codec only)
12-3	Slot 3-12 Valid bits as defined by AC '97
2	Reserved (Set to 0)
†1-0	2-bit Codec ID field (00 reserved for Primary; 01, 10, 11 indicate Secondary)
† New definitions for Secondary Codec Register Access	

Table 41. Secondary Codec Register Access Slot 0-Bit Definitions

C.3.1 "Atomic slot" treatment of Slot 1 Address and Slot 2 Data

Some confusion resulted from the AC '97 FAQ discussion of atomic slot behavior. The intention of the FAQ recommendation was to eliminate the possibility of a split transaction (where a valid address is transmitted in Slot 1 during one audio frame and its associated data in Slot 2 during a subsequent frame), not to relax the AC '97 Digital Controller requirements for Tag phase valid Slot signaling.

Command or Status Address and Data cannot be split across multiple AC-link frames. The following transactions require that valid Slot 1 Address and valid Slot 2 Data be treated as "atomic" (inseparable) with Slot 0 Tag bits for Address and Data set accordingly (that is, both valid): AC '97

- AC '97 Digital Controller write commands to Primary Codecs
- AC '97 Codec status responses

Whenever the AC '97 Digital Controller addresses a Primary Codec or an AC '97 Codec responds to a read command, Slot 0 Tag bits should always be set to indicate actual Slot 1 and Slot 2 data validity.

Function	Slot 0, bit 15 (Valid Frame)	Slot 0, bit 14 (Valid Slot 1 Address)	Slot 0, bit 13 (Valid Slot 2 Data)	Slot 0, Bits 1-0 (Codec ID)
AC '97 Digital Controller Primary Read Frame N, SDATA_OUT	1	1	0	00
AC '97 Digital Controller Primary Write Frame N, SDATA_OUT	1	1	1	00
AC '97 Codec Status Frame N+1, SDATA_IN	1	1	1	00

Table 42. Primary Codec Addressing: Slot 0 Tag Bits

When the AC '97 Digital Controller addresses a Secondary Codec, the Slot 0 Tag bits for Address and Data must be 0. A non-zero, 2-bit Codec ID in the LSBs of Slot 0 indicates a valid Read or Write Address in Slot 1, and the Slot 1 R/W bit indicates presence or absence of valid Data in Slot 2.

Function	Slot 0, bit 15 (Valid Frame)	Slot 0, bit 14 (Valid Slot 1 Address)	Slot 0, bit 13 (Valid Slot 2 Data)	Slot 0, Bits 1-0 (Codec ID)
AC '97 Digital Controller Secondary Read Frame N, SDATA_OUT	1	0	0	01, 10, or 11
AC '97 Digital Controller Secondary Write Frame N, SDATA_OUT	1	0	0	01, 10, or 11
AC '97 Codec Status Frame N+1, SDATA_IN	1	1	1	00

Table 43. Secondary Codec Addressing: Slot 0 tag bits

C.4 Clocking for Multiple Codec Implementations

Supporting multiple Codecs while also maintaining backwards-compatibility for AC '97 Codecs to be used as the primary Codec presents some challenges. A multiple Codec audio / modem configuration typically would want to target the highest quality audio while also supporting D3 cold wake-up modem capabilities. The quality concern mandates clean AVdd and DVdd voltage sources for the AC '97, while modem power management (D3 wake) capabilities dictates being powered by Vaux. Given this there may be cases when it may make sense to supply a free running high-speed clock to both Codecs. In this way all Codecs can be independently power managed without any problems that would be associated with being dependent on some other Codec's clock being active. The AC '97 Digital Controller could be designed to manage power to the source of the high-speed clock.

To keep the system synchronous the primary and secondary Codecs must be supplied with the SAME 24.576 MHz clock, so they are operating on the same time base. Regardless of the high-speed clock source, basing all AC-link timing on the BIT_CLK provided by the Primary Codec is necessary to insure that everything on the AC-link will be synchronous.

The following are potential clocking options available to a Secondary Codec:
1. Using a common external 24.576 MHz signal source (that is, external oscillator…see Figure 33)
2. Using the Primary's crystal out
3. Using a common external 24.576 MHz sourced by the AC '97 Digital Controller
4. Using the Primary's BIT_CLK output with a DPLL to derive 24.576MHz

See AC '97 2.1 Appendix D for updated audio and modem Codec clocking requirements.

When the AC-link is either programmed to the low power mode or shut off completely, BIT_CLK stops which shuts down the AC-link clock to the Secondary Codec[13]. In order for the Secondary Codec to react to an external event (phone ringing), it must support an independent clocking scheme for any PME# associated logic that must be kept alive when the AC-link is down. This includes logic to asynchronously drive SDATA_IN to a logic high-level which signals a wake request to the AC '97 Digital Controller.

[13] Secondary Codec always configures its BIT_CLK pin as an input.

Appendix D. AC ’97 2.1 Specification Updates

D.1 AC ’97 2.1 Audio

D.1.1 New Audio Definitions

The following sections discuss a number of new definitions, including several that affect pinout, such as external amplified powerdown (EAPD) functionality, LINE_OUT, HP_OUT, and consumer equipment (CE) compatible LNLVL_OUT, and Codec ID strapping.

The revised pin assignments for the 48-pin package are summarized as follows:

- LNLVL_OUT L,R: pins 39,41
- Codec ID0#,ID1# strapping: pins 45,46
- EAPD pin: pin 47
- Vendor specific: pin 48

D.1.1.1 External Audio Amplifier Control Bit and Pin

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
26h	Powerdown Ctrl/Stat	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	MDM	REF	ANL	DAC	ADC	na

AC ‘97 2.1 compliance ***requires*** the implementation of a dedicated output pin for external audio amplifier control. The pin is controlled via the newly re-defined “EAPD” (External Amplifier Power Down) bit in Powerdown Ctrl/Stat register 26h, bit 15 (formerly PR7). EAPD = 0 places a 0 on the output pin, enabling an external audio amplifier, EAPD = 1 shuts it down. Audio amplifier devices that operate with reverse polarity may require an external inverter.

The ***required*** pin assignment is to use pin 47 on the 48-pin package. The list of pins that are disabled in ATE test mode should include the external amplifier powerdown output pin.

Power-up default is EAPD = 0 (external audio amplifier enabled).

D.1.1.2 Line Out (Speaker), Headphone Out, True Line Out (CE)

AC ’97 1.03 defined output pins and independent volume controls for speaker output and an optional headphone output with integrated amplifier and 32 Ohm drive capability. The AC ’97 2.0 paragraph on “True Line Level Out” discussed the emerging requirement for two independent output levels, and recommended elimination of the integrated headphone amplifier for general purpose AC ’97 Codecs.

AC ‘97 2.1 compliance ***requires*** providing two stereo outputs with non-interdependent volume operation:

- LINE_OUT with volume control via register 02h (L, R pins 35,36 for 48 pin package)
- LNLVL_OUT (a.k.a. HP_OUT) with either fixed output level or ***optional*** volume control via register 04h (L,R pins 39,41 for 48-pin package)

This will meet system designers’ needs for most desktop or mobile systems:

- Speaker out with master volume control (register 02h) and off-chip amplification using LINE_OUT
- Headphone out with master volume control (register 02h) and off-chip amplification using LINE_OUT
- Consumer electronics (CE) compatible line out at a fixed (or fixable) ~1 Vrms for desktop (~0.7 Vrms for 3.3V mobile systems) using LNLVL_OUT

This requirement supports desktop PCs with external speaker and headphone jacks controlled by the same master volume, plus an independent CE-compatible external line level out. Muting the amplified speaker output during headphone use can be implemented physically via jack insertion switching (or possibly via vendor-specific software

detection of insertion plus control of the External Amplifier Powerdown (EAPD) pin). This requirement supports mobile PCs with internal speakers and external speaker and/or headphone jacks controlled by the same master volume, plus an independent CE-compatible external line level out.

For desktop or mobile systems that do not require a fixed CE-compatible external line level out, LNLVL_OUT with the optional volume control via register 04h can function as an independent HP_OUT (using an external amplifier) and support independent speaker and headphone volumes.

AC ‘97 2.1 compliance ***requires*** that vendors adopt the following method for detecting presence or absence of support for LNLVL_OUT with optional volume control via register 04h:

If the Reset ID4 bit (register 00h, bit 4) default value (following cold or warm reset) reads 1, then LNLVL_OUT is supported. If Headphone Volume (register 04h) default value (following cold or warm reset) reads 0000h, then the optional volume control is not supported.

Note that the Line Level Output may be powered down through bit PR6 in register 26h.

D.1.1.3 Elimination of the On-board Audio Speaker

PC systems currently rely on an internal speaker for PC_BEEP monitoring. Routing the PC_BEEP signal to the system speakers enables cost reduction via elimination of the redundant speaker. PC_BEEP is used in the pre-boot environment for POST error reporting. As long as analog is present in the system there is an option to route PC_BEEP through the system audio Codec or external audio amplifier device. Since PC_BEEP is a pre-boot, analog-connected signal, supporting similar functionality for USB speakers will be more challenging – it potentially requires changes to the core logic, and some level of pre-boot USB audio device enumeration and support.

The AC '97 technical FAQ originally published in September 1996 described in detail how to route PC_BEEP through the AC ’97 Codec mixer. This discussion is reproduced below.

> *PC_BEEP supports motherboard AC ‘97 Controller /Codec implementations. The intention of routing PC_BEEP through the Codec analog mixer is to eliminate the requirement for an onboard speaker or piezoelectric device by guaranteeing a connection to speakers connected via the output jack. In order for this to be viable the PC_BEEP signal needs to reach the output jack at all times, with or without the audio driver's support.*
>
> *The Primary sources of PC_BEEP are:*
> - *Power On Self Test (POST) error reporting (at system boot time before the audio driver has loaded)*
> - *Windows system alerts (when no audio driver is installed)*
> - *DOS applications which make BIOS calls or write directly to IO port 61 (independent of audio driver)*
>
> *The AC `97 Component Specification recommends a passive connection between PC_BEEP and LINE_OUT_L/R whenever the AC-link RESET# is held active low. PC_BEEP for POST error reporting can be guaranteed if the AC `97 Controller holds AC-link RESET# low until after the AC ‘97 Controller is first accessed (by BIOS) following a cold reset. It may also be possible to enable the passive PC_BEEP connection whenever the AC '97 mixer is in power-down state (this is an option left up to the IHV).*

The following is one possible power on sequence which supports the PC_BEEP passive connection:

1. Cold reset	*1. AC ‘97 Controller powers up.*
2. BIOS performs POST	*2. During this stage the AC ‘97 Controller holds AC-link RESET# active low, and the PC_BEEP passive connection is enabled, allowing POST CODES to pass to the speakers.*
3. BIOS begins PnP	*3. BIOS PnP configures AC '97 Controller legacy & native PCI audio device(s). AC ‘97 Controller de-asserts RESET# and begins Codec initiation sequence. PC_BEEP switchover from passive to active begins. BIOS completes AC ‘97 Controller PnP config and moves on without waiting for AC '97 Codec to be fully powered on.*
4. BIOS completes PnP	*4. AC '97 Codec completes power up (0-500ms later), AC ‘97 Controller completes legacy device initialization, including unmuting the AC ‘97 mixer master volume. Legacy audio is now ready.*
5. DOS prompt	*5. PC_BEEP through AC ‘97 Codec mixer enabled.*
6. Win 95 loads	*6. Win 95 AC ‘97 driver loads and initializes native PCI device(s).*

Care should be taken to avoid the introduction of a pop when powering the mixer up or down, and that the above described functionality for the passive PC_BEEP connection does not jeopardize the audio quality of LINE_OUT (i.e., introduce unwanted noise). Support for this feature should not come at the expense of the AC ‘97 quality goals, the OEM has the option to route PC_BEEP external to the AC ‘97 Codec.

D.1.2 Audio Codec Cost Reduction Options

As audio features migrate to digital, some of the original baseline AC ’97 features may not be needed in future products. In general, if a feature/function is not implemented the following detection protocol can be used:

1. Write all 1's to the appropriate AC ’97 register or bit field
2. If the register or bit field read-back value reads 0, the function is not implemented

AC ’97 2.1 defines the following analog mixer features as ***optional*** to implement, and AC ‘97 2.1 compliance ***requires*** (for interoperability reasons) that vendors develop Controllers and drivers which specifically test for presence or absence of support for these features:

- MONO_OUT (register 06h, default 8000h)
- PC_BEEP (register 0Ah, default 0000h)
- PHONE (register 0Ch, default 8008h)
- VIDEO (register 14h, default 8808h)
- AUX (register 16h, default 8808h)
- MIC2 (register 20h, bit 8, default 0)

D.2 AC '97 2.1 Modem

D.2.1 New Modem Definitions

D.2.1.1 Elimination of the On-board Modem Speaker

Modem subsystems currently rely on an on-board speaker for call progress monitoring. Routing call signals through the system speakers enables cost reduction via elimination of the redundant speaker. There is a hardware-dependent analog solution and a hardware-independent digital solution (which supports analog or USB speakers).

- Analog solution: The system designer can route an analog mix of the modem Tx and Rx signals through PHONE input of the AC '97 analog mixer. This requires that the modem control task have access to AC'97 audio driver interface PHONE volume and mute controls, and introduces a dependency on the user's preferred master audio volume and mute settings[14] (which the modem driver should not attempt to access).

- Digital solution: The modem driver designer can route digital copies of the modem Rx (ADC) and Tx (DAC) streams (or perhaps just the digitized pre-echo-canceled modem Rx stream from the ADC) into the system-wide software audio mixer. As with the analog solution, this introduces a dependency on the user's preferred master audio volume and mute settings. For this technique to be cost-effective a soft modem implementation is probably required.

For soft modem implementations AC '97 2.1 ***recommends*** the digital call progress monitoring solution[15].

D.2.2 Modem Codec Cost Reduction Options

D.2.2.1 Required Sample Rates

AC '97 2.1 compliance ***no longer requires*** support for modem sample rates of 24 and 48 kHz. AC '97 2.1 ***recommends*** that the default modem sample rate (following cold or warm reset) be the highest sample rate supported.

D.2.2.2 Internal PHONE and MONO_OUT Connections (AMC '97)

The AC '97 PHONE input was designed to support monitoring of analog telephony signals, such as speakerphone or call progress, through the audio subsystem and speakers. The AC '97 MONO_OUT was designed to support routing of analog system audio signals (PHONE and PC_BEEP excluded) to the modem subsystem.

Prior to controllerless modems and low latency digital audio, support for voice required:
a) controller functionality to encode and decode digital voice data
b) a dedicated voice Codec
c) analog connections between the modem and audio subsystems

Current voice modem implementations migrate the controller functionality into the modem driver, eliminate the redundant voice Codec, and rely on low latency digital streaming between the modem and audio drivers.

For backward compatibility reasons, including support for legacy operating systems that will still be shipping in 1999, it is probably premature to eliminate support for the AC '97 PHONE and MONO_OUT analog interconnections. However, AMC designs may ***optionally*** implement the PHONE and MONO_OUT connections internally to save package pins. For certification reasons, care should be taken to limit the bandwidth of analog audio signals coupled to the modem Tx via MONO_OUT.

---

[14] In the Win32* Driver Model (WDM), access to the analog mixer topology is provided via SysAudio interface calls. These calls allow access to mixer mute/volume controls and eliminate the need for a proprietary audio driver interface. Refer to the Audio Device Class Reference Specification available from Microsoft.

[15] The digital solution isolates the final call progress rendering hardware. The analog solutions do not lend themselves easily to audio upgrades or the use of USB speaker solutions. Refer to the Audio Device Class Reference Specification available from Microsoft.

D.3 AC '97 2.1 Multiple Codec Definitions

D.3.1 Multiple Codec Clocking Requirements

D.3.1.1 Primary AC, MC, or AMC Codec

Primary AC/MC/AMC devices are ***required*** to function correctly using either of the following clocking options:

a) 24.576 MHz crystal attached to XTAL_IN and XTAL_OUT
b) 24.576 MHz external oscillator provided to XTAL_IN

D.3.1.2 Secondary AC Codec

Secondary AC devices are ***required*** to function correctly using one or more of the following clocking options:

a) 24.576 MHz external oscillator provided to XTAL_IN (synchronous with Primary)
b) the BIT_CLK input provided by the Primary

D.3.1.3 Secondary MC Codec

Secondary AC/MC/AMC devices are ***required*** to function correctly using one or more of the following clocking options:

a) the BIT_CLK input provided by the Primary
b) a vendor specified crystal attached to XTAL_IN and XTAL_OUT
c) 24.576 MHz external oscillator provided to XTAL_IN (synchronous with Primary, optionally 3.3Vaux powered)

Regardless of clocking option, Secondary MC Codecs are ***required*** to observe AC-link timing synchronous with their BIT_CLK and SYNC inputs. Secondary MC Codecs which utilize clocking option a) during full power states have a dependency on the accuracy and stability of the BIT_CLK sourced by the Primary AC Codec. Secondary MC Codecs which support wake-up/Caller-ID functionality are dependent on option b) or c) at least during 3.3Vaux powered states. The choice of clocking options b) vs. c) can have an impact on sleep state power consumption.

D.3.2 Multi-channel Audio using Multiple Audio Codecs

AC '97 2.1 defines ***optional*** support for default mapping of AC-link output slots to 2-channel audio DAC functions based on Codec ID. This makes it easier to develop interoperable multi-channel implementations using multiple 2-channel AC '97 2.1 Codecs. AC '97 2.1 also ***recommends*** a synchronization technique for Controllers which do support multi-channel output.

D.3.2.1 Slot to DAC Mappings for Multi-channel Audio Output

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
28h	Extended Audio ID	ID1	ID0	x	x	x	X	AMAP	LDAC	SDAC	CDAC	x	x	VRM	x	DRA	VRA	xxxxh

The AMAP bit, D9 in the Extended Audio ID Register (register 28h), indicates whether or not the audio Codec supports ***optional*** AC '97 2.1 compliant AC-link slot to audio DAC mappings. AMAP = 1 in D9 indicates that the default (following cold or warm reset) Codec slot to DAC mappings (configured via hardwiring, strap pin(s), or other methods) conform to Table 44.

Codec ID	AC-link Frame Data Used for DACs		Comments
	PCM Left DAC uses data from Slot #	PCM Right DAC uses data from Slot #	
00	3	4	Original definition (master)
01	3	4	Original definition (docking)
10	7	8	Left/Right surround channels
11	6	9	Center/LFE channels
The Codec ID is available to the Controller via register 28h, bits D15 & D14.			

Table 44. Default Slot to DAC Mappings Based on Codec ID

D.3.2.2 Synchronization for Multi-channel Audio Output

To establish channel synchronization across multiple audio Codecs at the beginning of playback, AC '97 2.1 ***recommends*** that a multi-channel Controller tag all outgoing slots "invalid" until data is ready to be sent for all channels, then provide the first "valid" data to all active output slots during the same AC-link frame.

D.4 AC '97 2.1 Power Management

D.4.1 Power Management "D State" Mappings for Audio Codecs

The ACPI and PCI Bus Power Management Interface specifications define a standard set of device power management states (D0 – D3). An audio device driver written to comprehend these power management specifications must map each supported system-side D state to an audio Codec-specific power savings mode using the PR bits.

A high-level set of expectations for the mapping of D States to audio feature availability, power consumption, resume latency, etc., is available in the Audio Device Class Power Management Reference Specification located at:

http://www.microsoft.com/hwdev/download/audpmspc.rtf

Table 45 details a lower-level mapping of the audio subsystem D states to the recommended AC'97 Codec power savings PR settings.

	PR<0:7>								+12 Vmain	+5Vaa from +12 Vmain	+3.3 Vmain	+3.3 Vaux	Comments
	EAPD	HP Amp	Int. CLK	AC-Link	Mixer Vref	Mixer	DAC	ADC					
Device State	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**					
D0	0	0	0	0	0	0	0	0	On	On	On	On	All on
D1	0	0	0	0	0	0	***1***	***1***	On	On	On	On	-DAC, -ADC
D2	***1***	0	0	0	0	***1***	1	1	On	On	On	On	-Mix, -Amp
$D3_{hot}$	1	***1***	***1*** Note 3	0 Note 1	1/0 Note 2	1	1	1	On	On	On	On	-int clk -hp amp
$D3_{cold}$	-	-	-	-	-	-	-	-	Off	Off	Off	On	unpowered

Table 45. Recommended Audio Codec D state to PR bit mapping

Note 1: PR4 (AC-link BIT_CLK stopped), is not recommended for $D3_{hot}$. Under certain circumstances disabling of the AC-link BIT_CLK during $D3_{hot}$ may interfere with Secondary modem Codec operation, and so is not recommended. For details on this clocking issue refer to Section D.4.3.5.

Note 2: Disabling of Vref (i.e., PR3 = 1) will impose a hardware-dependent power-up delay upon resuming. An audio vendor must weigh the incremental power savings that setting PR3 brings, against the added resume latency it imposes when deciding how the audio driver is to treat this bit while preparing to enter $D3_{hot}$.

Note 3: The PR5 bit is intended to enable a Primary AC Codec to enter its lowest power internal state while still providing BIT_CLK to Secondary Codecs on the AC-link. Depending on how PR5 is implemented, AMC or AC + MC designs may need to manage PR5 identically to PR4.

When the system transitions to a deep sleep state of S3, S4 or S5, all main voltage rails are shut off leaving the audio Codec unpowered. During each transition to $D3_{hot}$, the audio driver must assume that it will ultimately end up in $D3_{cold}$, and as such, must save off all internal state, and functional context that would be needed to resume correctly from the $D3_{cold}$ unpowered state.

D.4.2 Power Management "D State" Mappings for Modem Codecs

The ACPI and PCI Bus Power Management Interface specifications define a standard set of device power management states (D0 – D3). A modem device driver written to comprehend these power management specifications must map each supported system-side D state to a modem Codec-specific power savings mode using the PR bits.

A high-level set of expectations for the mapping of D States to modem feature availability, power consumption, resume latency, etc., is available in the Communications Device Class Power Management Reference Specification located at:

http://www.microsoft.com/hwdev/download/compmspc.rtf

Table 46 details a lower-level mapping of the modem subsystem D states to the recommended MC '97 Codec power savings PR settings.

PR<A:D> + MLNK (1-line modem Codec example)						+12 Vmain	+5Vaa from +12Vmain	+3.3 Vmain	+3.3 Vaux	Comments
	AC-Link	DAC1	ADC1	Vref	GPIO					
Device State	MLNK	D	C	B	A					
D0	0	0	0	0	0	On	On	On	On	All on
D1	0	***1***	***1***	0	0	On	On	On	On	-DAC, -ADC
D2	0	1	1	0	0	On	On	On	On	Same as D1
$D3_{hot}$	***1*** Note 1	1	1	Note 2	Note 2	On	On	On	On	-AC-Link
$D3_{cold}$	-	-	-	Note 2	Note 2	Off	Off	Off	On	3.3Vaux power only

Table 46. Recommended Modem Codec D state to PR bit mapping

Note 1: Codec behavior, with respect to its MLNK bit being set, is dependent upon whether the modem Codec was configured as the primary or secondary Codec. Refer to Section D.4.3.1.

Note 2: GPIO (PRA) bit must be 0 to enable wake-on-ring functionality. If caller ID is supported, to enable caller ID capture the Vref (PRB) bit must also be 0.

Note 3: If a modem Codec is configured as the Primary AC-link Codec, there should not be any audio Codecs residing on the AC-link (i.e., a modem-only configuration is the only supported configuration for MC '97 as the primary AC-link Codec).

D.4.3 Power Management with Wake-up Capabilities

D.4.3.1 Clarification of MLNK and AC-link Powerdown

AC '97 2.0 defined the modem MLNK bit as a flag which, when set, indicates to the modem Codec that the AC-link is about to be placed in a low power mode with BIT_CLK stopped.

In a typical AC + MC, or AMC configuration the audio Codec is deployed as the Primary Codec, and the modem Codec is deployed as the Secondary Codec. Setting the MLNK bit, given one of these common configurations is problematic. The issue is that there is no standard mechanism for the modem driver to know when the audio driver is about to program the audio Codec to PR4, and so when it should set the MLNK bit. The audio and modem drivers must remain mutually exclusive of each other. Therefore the MLNK bit, in any audio/modem configuration with the modem Codec deployed as the secondary Codec is meaningless as specified in AC '97 2.0.

New MLNK bit Definition:

Miscellaneous Modem Status and Control Register (56h) Bit 12.

MLNK indicates to the modem Codec that its modem driver is preparing the modem subsystem to enter the $D3_{hot}$ state.

The modem Codec's behavior following the setting of its MLNK bit is dependent upon whether the Codec has been configured as the primary or secondary AC-link Codec.

D.4.3.1.1 Primary MC'97 Codec and MLNK

Setting the MLNK bit must cause an AC-link halt condition (BIT_CLK stays at a logic low level). At the same time the modem Codec must also drive and hold its SDATA_IN signal low. This is similar to setting the PR4 bit for a primary AC '97 audio Codec.

Once the MLNK bit has been set by its modem driver, BIT_CLK and SDATA_IN must remain at a logic low level until one of three things happen:

1. Low to high transition of RESET# on the AC-link
2. Warm Reset sequence signaled on the AC-link
3. A power management event occurs, such as a ring detection (pertains to SDATA_IN only)

The low to high transition of AC-link RESET# indicates resumption from the $D3_{cold}$ state where AC-link power had been removed. The sampling of this transition on the RESET# signal must effectively be treated as if observing a warm reset in the sense that no internal auxiliary powered state logic is impacted (i.e., reinitialized). Unaffected logic must include, but not necessarily be limited to, wake event status and caller ID data if supported. Resumption of normal AC-link activity must begin as though the Codec had been issued a warm reset semantic.

Warm Reset is the required resume sequence had the modem Codec been resumed from a $D3_{hot}$ state where the AC-link had been halted yet full power had been maintained. If the modem Codec observes a Warm Reset sequence (i.e., SYNC assertion in the absence of BIT_CLK) the modem Codec shall reactivate the AC-link in the manner specified in Section 5.2.1.2.

If the modem Codec has been enabled to wake the system, and a power management event occurs (such as the phone ringing), then the modem Codec complies with the behavior specified in Section B.5.

D.4.3.1.2 Secondary MC'97 Codec and MLNK

Setting the MLNK bit when transitioning a secondary modem Codec to the $D3_{hot}$ state requires different behavior from the modem Codec than what is required from a primary modem Codec.

The potential for subsequent primary audio Codec activity requires that a secondary modem Codec must continue to be an active participant on the AC-link so long as the AC-link continues to transact I/O frames. If enabled to generate a wake event while MLNK is set yet the AC-link is still transacting I/O frames, the modem Codec must pass the GPI (Ring Indication) information normally over its SDATA_IN signal within slot 12.

If the AC-link is programmed to a PR4[16] (AC-link halted with BIT_CLK held low) the Codec must be able to detect this and must, upon detecting this, drive and hold its SDATA_IN signal low. If enabled to wake on ring the appropriate GPI assertion shall cause the modem Codec to transition its SDATA_IN signal from low to high signaling the wake request.

If the AC-link is transitioned to a $D3_{cold}$ state (i.e., power removed) subsequent to the MLNK bit having been set , the modem must drive and hold its SDATA_IN signal low. If enabled to wake on ring the appropriate GPI assertion shall cause the modem Codec to transition its SDATA_IN signal from low to high signaling the wake request.

[16] Not recommended for multiple, audio + modem, Codec configurations. See Section D.4.3.5.

Detecting that the AC-link has transitioned to the $D3_{cold}$ state may be accomplished by sampling the AC-link RESET# signal, given that whenever the AC-link is in the $D3_{cold}$ state RESET# is required to be actively asserted.

Once the modem Codec's SDATA_IN has been driven low for one of the two aforementioned reasons, it must remain at a logic low level until one of three things happen:

1. Low-to-high transition on AC-link RESET#
2. Warm Reset sequence signaled on the AC-link
3. A power management event occurs, such as a ring detection

The low-to-high transition of AC-link RESET# indicates resumption from the $D3_{cold}$ state where AC-link power had been removed. The sampling of this transition on the RESET# signal must effectively be treated as if observing a warm reset in the sense that no internal auxiliary powered state logic is impacted (i.e., reinitialized). Unaffected logic must include, but not necessarily be limited to, wake event status and caller ID data if supported. Resumption of normal AC-link activity must begin as though the Codec had been issued a warm reset semantic.

Warm Reset is the required resume sequence had the modem Codec been resumed from a $D3_{hot}$ state where the AC-link had been halted yet full power had been maintained. If the secondary modem Codec observes a Warm Reset sequence (i.e., SYNC assertion in the absence of BIT_CLK) the modem Codec shall resume normal internal operation and begin communicating over the AC-link when ready.

If the modem Codec has been enabled to wake the system, and a power management event occurs (such as the phone ringing), then the modem Codec shall comply with the behavior specified in Section B.5.

D.4.3.2 Warm and Cold AC-link Reset Considerations

AC-link reset operations occur when the system is initially powered up, when resuming from a lower powered sleep state, and in response to critical subsystem failures that can only be recovered from with a reset.

The following subsections focus on the behavior of the AC-link when resuming from a low power sleep state.

D.4.3.2.1 Resume Reset Behavior

The form of reset that is signaled (if necessary) when resuming the AC-link and its Codec(s) is dependent upon the state of the Codec(s), and the power management state of the system.

Table 47. Table 48, and Table 49 break down the AC-link behavior that must occur when resuming the AC-link as a function of audio Codec device state, modem Codec device state, and system state.

Audio Codec D-State	System State (ACPI: S0-S5)	Resume activity	Comments
D0	S0	N/A	Audio active; System is operating in the Working State
D1	S0 or S1	No reset; PR bits modified	Audio idle; System is either operating in the Working State or is in S1 sleep state
D2	S0, S1, or S2	No reset; PR bits modified	Audio idle; System is either operating in the Working State, or is in S1 or S2 sleep state
$D3_{hot}$	S0, S1, or S2	PR bits modified, preceded by a Warm Reset if PR4 was set	Audio idle; System is either operating in the Working State, or is in S1 or S2 sleep state
$D3_{cold}$	S3, S4, or S5	Cold Reset; full Codec register and context restoration	Deep sleep state; no power to audio Codec

Table 47. Resume Reset Behavior: Audio-only

Modem Codec D-State	System State (ACPI: S0-S5)	Resume activity	Comments
D0	S0	N/A	Modem active; System is operating in the Working State
D1	S0 or S1	No reset; PR bits modified	Modem idle; System is either operating in the Working State or is in S1 sleep state
D2	S0, S1, or S2	No reset; PR bits modified	Modem idle; System is either operating in the Working State, or is in S1 or S2 sleep state
$D3_{hot}$	S0, S1, or S2	PR bits modified, preceded by a Warm Reset if MLNK was set	Modem idle; System is either operating in the Working State, or is in S1 or S2 sleep state
$D3_{cold}$	S3, S4, or S5	Cold reset to AC-link; modem Codec must interpret this as a warm reset; full audio Codec register and context restoration, modem Codec may need partial context restoration	Deep sleep state; only auxiliary power available to the modem Codec; modem may be armed to answer the phone (except when in ACPI S5)

Table 48. Resume Reset Behavior: Modem-only

Audio Codec D-State	Modem Codec D-State	System State (ACPI: S0-S5)	Resume activity	Comments
D0	D0	S0	N/A	Audio/Modem active; System is operating in the Working State
D0	D1, D2 or $D3_{hot}$	S0	No reset; modem Codec PR bits modified	Audio active, Modem idle; System is operating in the Working State
D1	D0	S0	No reset; audio Codec PR bits modified	Audio idle, modem active; System is operating in the Working State
D1	D1, D2 or $D3_{hot}$	S0 or S1	No reset; audio and modem PR bits modified	Both Codecs idle; System is either operating in the Working State or in the S1 sleep state
D2	D0	S0	No reset; audio Codec PR bits modified	Audio idle, modem active; System is operating in the Working State
D2	D1, D2 or $D3_{hot}$	S0, S1, or S2	No reset; audio and modem Codec PR bits modified	Both Codecs idle; System is either operating in the Working State, or in the S1 or S2 sleep state
$D3_{hot}$	D0	S0	No reset; audio Codec PR bits modified	Audio Codec idle, modem active; System is operating in the Working State (note audio Codec PR4 is prohibited in Codec/system state as it would preclude normal secondary modem Codec operation)
$D3_{hot}$	D1, D2 or $D3_{hot}$	S0, S1, or S2	Warm Reset if audio PR4 bit is set; otherwise audio and modem PR bits modified only	Both Codecs idle; System is either operating in the Working State, or in the S1 or S2 sleep state
$D3_{cold}$	$D3_{cold}$	S3, S4, or S5	Cold reset to AC-link; modem Codec must interpret this as a warm reset; full audio Codec register and context restoration, modem Codec may need partial context restoration	Deep sleep state, no power to audio Codec, only auxilairy power to modem; modem may be armed to answer the phone (except when in ACPI S5)

Table 49. Resume Reset Behavior: Audio and Modem

D.4.3.2.2 Resuming Normal AC-link Operation from S3, S4 or S5 System Sleep State

In accordance with prior revisions of the AC '97 specification, when the AC-link is unpowered, as is the case when the system is in either S3, S4 or S5, the AC-link RESET# output buffer is unpowered typically leaving the RESET# signal floating at or near ground. Given the low active nature of AC-link RESET#, this presents a problem for modem Codecs that must continue to operate under auxiliary power while the system sleeps. An auxiliary powered modem Codec could be faced with what would appear to it as a perpetual reset condition.

This issue is identical to the problem that any PCI-based $D3_{cold}$/PME# capable function faced when the PCI bus was programmed to B3 and the PCIRST# output buffer, being unpowered, floated around ground potential. Prior to the 3.3Vaux PCI-PM Specification updates, which require PCIRST# to be actively asserted whenever the PCI bus was in the unpowered B3 state, these PCI functions had no way of knowing for certain whether or not a real reset had occurred or whether the bus was unpowered and floating near ground potential.

AC-link RESET# SIGNALING REQUIREMENT

AC-link RESET# must be asserted, and actively held low whenever the system is in the S3, S4 or S5 state. Given this DC '97 Controller guarantee that the AC-link RESET# signal remains low at these times, an auxiliary powered modem Codec can use the low-to-high transition on RESET# as a reliable indication that power has been reestablished on the AC-link, and that an actual resume reset has occurred.

An AC '97 2.1 Controller/Codec arrangement deployed as a PCI add-in card could have its AC-link RESET# signal follow the PCIRST# signal directly since PCIRST# will always be asserted whenever the system is sleeping in S3, S4 or S5.

D.4.3.3 Power Distribution

The AC '97 Revision 1.03 architecture was intended to enable low cost, yet high performance audio Codecs by establishing a standard split of the digital and analog portions of the audio subsystem. AC '97 Revision 2.0 brought low cost, and flexible integration of a modem Codec to the AC-link as well. The AC '97 Revision 2.1 architectural enhancements and clarifications are intended to, among other things, help merge the two subsystems with the ACPI-based Instantly Available PC power management initiative.

The desired result in applying Instantly Available PC technology to the audio and modem subsystems is to maintain AC '97's high audio quality, while not compromising an AC-link modem Codec's ability to wake the system from a very low power, deep sleep state. To meet these objectives audio designers must have the ability to derive locally, a tightly regulated Vref supply for the Codec's DACs and ADCs. At the same time the modem Codec must have auxiliary power available to them so that they may alert the system of a ringing phone even from an ACPI S3, or S4 sleep state where 95% of all PC power is shut off.

For more detail on Instantly Available PC power terminology and specifications refer to the "Instantly Available PC Power Delivery Requirements and Recommendations" Specification, which can be downloaded from:

http://developer.intel.com/design/power/supply98.htm

The following subsections detail Instantly Available PC power distribution requirements for what is expected to be the three predominant AC '97 2.1 configurations.

D.4.3.3.1 MC '97 (Primary) Implementations

In support of an Instantly Available PC's "Off-yet Communicating" capabilities, modem Codecs must be capable of waking the system from a sleep state wherein the main power rails have been shut off. This implies the usage of auxiliary power.

Table 50 illustrates, all AC-link signals driven from the modem Codec, as well as all modem Codec circuitry (both digital and analog) must be powered by an auxiliary 3.3 V supply (3.3 Vdual).

	+3.3Vmain	+5Vmain	+12Vmain	+3.3Vdual(3.3Vaux)
AC-link (Codec outputs)				
■ BIT_CLK				✓
■ SDATA_IN				✓
AC-link (contrl. outputs)				
■ SYNC	✓			
■ SDATA_OUT	✓			
■ RESET#				✓
MC'97 digital logic				✓
MC'97 analog circuitry				✓ (note 1)

Table 50. Power Distribution: MC '97 as the Primary (Modem-Only configuration)

Note 1: Modem codecs that do not support hardware capture of caller ID during ACPI S3 or S4 states may alternatively power their analog circuitry with either 3.3Vmain or 5Vmain.

D.4.3.3.2 AC '97 (Primary) + MC '97 (Secondary) Implementations

Table 51 depicts the power distribution that enables both high quality audio and "Off-yet Communicating" modem operation.

	+3.3Vmain	+5Vmain	+5Vaa from +12Vmain	+3.3Vdual(3.3Vaux)
AC-link (Codec outputs) ■ BIT_CLK ■ SDATA_IN(audio) ■ SDATA_IN(modem)	 ✓ ✓			 ✓
AC-link (contr. outputs) ■ SYNC ■ SDATA_OUT ■ RESET#	 ✓ ✓			 ✓
Audio digital logic	✓			
Audio analog circuitry		✓ (mobile option)	✓	
Modem digital logic				✓
Modem analog circuitry				✓ (note1)
Modem wake logic				✓

Table 51. Power Distribution: Split Codec Partitioned Audio-plus-Modem

Note 1: Modem codecs that do not support hardware capture of caller ID during ACPI S3 or S4 states may alternatively power their analog circuitry with either 3.3Vmain or 5Vmain.All audio Codec driven AC-link signals, as well as all other digital logic associated with the audio subsystem, must be powered by 3.3Vmain.

All modem Codec driven AC-link signals, as well as all other digital logic and analog caller ID capture circuitry must be powered by +3.3Vdual, enabling an Instantly Available PC.

It is recommended that the audio subsystem locally regulate +12Vmain down to +5Vaa for use by its analog circuitry.

This power distribution scheme enables the audio Codec to be powered from standard working state voltage sources that are shut off when the PC enters an ACPI sleep state of S3, S4 or S5. Additionally it enables the modem Codec to power its wake logic when in an S3, S4 or S5 ACPI sleep state.

D.4.3.4 Power Distribution: AMC '97 (Primary) Implementations

The AMC '97 combination Codec must implement the same power distribution strategy as for the split partitioned AC + MC Codec configuration. This imposes a requirement on AMC '97 Codec designs, in that they are designed with split power wells enabling multi-voltage power distribution for different sections of the component. Please refer to Table 51.

D.4.3.5 Multiple Audio + Modem Codec clocking considerations

In an AC '97 2.0 compliant multiple audio + modem Codec configuration[17] the AC '97 digital controller and Secondary modem Codec depend upon the Primary audio Codec delivering BIT_CLK to them for proper modem operation.

Therefore when the modem is in the active state (i.e., D0) the audio driver must never shut off the BIT_CLK by setting the audio Codec PR4 bit. To further complicate matters the audio and modem drivers must be mutually

[17] An AC '97 audio Codec with a physically separate MC '97 modem Codec or, a combined AMC '97 audio/modem Codec.

exclusive of each other, meaning that the audio driver is limited to managing the audio Codec hardware only and must not interact directly with the modem driver or modem Codec hardware. To avoid this BIT_CLK clocking issue it is recommended that the audio Codec PR4 bit NOT be set in multiple audio + modem Codec configurations.
AC '97 2.1 Multiple Codec Clocking ***Recommendations***:

1. An audio driver should never set the PR4 bit in a multiple audio + modem Codec configuration. This ensures that the BIT_CLK never stops when the PC is in the working state.
2. Primary Codecs accept either a series XTAL or Oscillator input of frequency 24.576 MHz.
3. Secondary Codecs use BIT_CLK (and SYNC) input for all AC-link transaction timings
4. Secondary modem Codecs should support an additional, auxiliary powered clock input (XTAL or OSC) that is used for hardware caller ID functionality while the system is in an ACPI S3, S4 or S5 sleep state (i.e., for use at times when the AC-link, including BIT_CLK, is powered off)

Audio-only multiple Codec implementations have no BIT_CLK clocking issues as all of the AC-link Codecs are managed by the same device driver.

D.4.4 Resume Latency: Device Driver Considerations

Device drivers should be written to distinguish between a cold boot, and a resume event from S3, S4 or S5. By making this distinction a driver could be written to minimize its contribution to the system's resume latency.

Device drivers should not use the same boot time initialization code sequence when resuming from S3, S4, or S5 sleep states.

D.5 AC ’97 2.1 Interoperability Requirements and Recommendations

D.5.1 Digital SRC in Controller or Codec

AC ’97 2.1 ***recommends*** that the digital SRC capability located in the AC ’97 Controller or AC ’97 2.x Codec meet the equivalent of the analog performance characteristics specified in Chapter 10.

AC ‘97 2.1 compliance ***requires*** that the digital SRC capability located in the Controller, Codec, or software driver meet or exceed the following for 44.1 kHz source output material (such as a 44.1 kHz wave file with a full scale swept digital sin wave, or Red Book content streamed from an audio CD):

- ≥85 dB FS A dynamic range (SNR)
- ≥17.64 kHz (0.4 Fs) -3 dB frequency response
- ≤-65 dB FS passband THD+N
- ≤0.5 dB passband ripple

D.5.2 Codec

D.5.2.1 Codec ID

To reserve unassigned Input Slot 0 bits for future expansion, AC ’97 2.1 ***recommends*** that Codecs configured as Secondary return 0s on SDATA_IN, Slot 0, bits 1 and 0 (NOT Codec ID). Since Codec ID can be read from the Extended Audio register (28h) or the Extended Modem register (3Ch) after a reset or other system state change (such as a docking event), there is no need to transmit Codec ID on every AC-link frame.

AC ’97 2.1 ***recommends*** that 2-channel audio Codecs in the 48-pin package which use strapping pins to configure the Codec ID use pins 45 and 46 as ID0# and ID1#. AC '97 2.1 ***recommends*** that the ID0# and ID1# strapping bits adopt inverted polarity and default to 00 = Primary (via internal pullup) when left floating. This eliminates external pulldown resistors for Codecs configured as Primary, and maintains backward compatibility with existing layouts that treat pins 45,46 as "no connect" or cap to ground.

ID1# (pin 46)	ID0# (pin 45)	Configuration
NC	NC	Primary
NC	pulldown	Secondary ID 01
pulldown	NC	Secondary ID 10
pulldown	pulldown	Secondary ID 11

Table 52. Recommended Codec ID strapping

D.5.2.2 Codec Register Status Reads

The following are AC ‘97 2.1 compliance ***requirements*** for registers outside of the vendor-defined space (5Ah-7Ah), and AC ’97 2.1 ***recommendations*** for registers within the vendor-defined space. Driver authors should assume nothing about vendor-defined space until they have confirmed the manufacturer and revision (registers 7Ch-7Eh) of the Codec being driven.

- **Non-implemented Register Bits:** All reserved or non-implemented register bits (marked x in the tables) are ***required*** to return 0 when read.
- **Non-implemented Addresses:** Read access to non-implemented registers are ***required*** to echo a ‘valid’ 7-bit register address in Input Slot 1 and return ‘valid’ 0000h data in Input Slot 2 on the next AC-link frame.
- **Odd Register Addresses:** Read (and write) access to odd register addresses are ***required*** to be treated the same as non-implemented addresses, instead of aliasing them to the next lower even-numbered register.

This is a change to the behavior specified in the AC ’97 2.0 Extended Register Map spec, where it was stated that:

> *AC ’97 2.0 Codecs should ignore accesses of odd-numbered registers instead of aliasing them to the next lower even-numbered register.*

D.5.2.3 Codec Register Status Read Completion Latency

For maximum Controller/Codec interoperability AC ‘97 2.1 compliance ***requires*** that Codec register read data be returned in the next AC-link frame following the frame in which the read request occurs.

This tightens the behavior described in the AC ’97 Technical FAQ, originally published in September 1996, which stated the following:

> *We are not requiring that the read requests be completed by the immediately following frame. For some functions this may not be possible. Valid return data for a given input frame is indicated by the tag associated with the Status Address Port being valid. As discussed, the combination of the Status Address and Status Data Ports should be treated as single atomic slot. The data returned within the Status Address Port echoes the register address for which the data in Status Data Port corresponds to. AC ‘97 Controllers should check the return address. While “out of order” reads are not specified, and “in order” reads are expected to be the norm, there may be cases where it makes sense to return readily available data out of order.*

D.5.2.4 The Codec-Ready Bit and Audio or Modem DAC/ADC Status Bits

AC ‘97 2.1 compliance ***requires*** that Codec-Ready and audio or modem DAC/ADC status bits only change from “ready” to “not ready” in response to a PR state change issued by the Controller to the Ctrl/Stat registers 26h, 2Ah, or 3Eh. This guarantees that once data is actively flowing on a slot, the Controller does not have to continuously read the Ctrl/Stat registers to detect any unexpected Codec PR status change.

D.6 AC '97 2.1 Electrical Characteristics

D.6.1 3.3 Volt DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Power Supply	Vdd	3.135	3.3	3.465	V
Input voltage range	V_{in}	-0.30	-	DVdd + 0.30	V
Low level input voltage	V_{il}	-	-	0.35 x Vdd	V
High level input voltage	V_{ih}	0.65 x Vdd	-	-	V
High level output voltage	V_{oh}	0.90 x Vdd	-	-	V
Low level output voltage	V_{ol}	-	-	0.10 x Vdd	V
Input Leakage Current (AC-link inputs)	-	-10	-	10	uA
Output Leakage Current (Hi-Z'd AC-link outputs)	-	-10	-	10	uA
Output buffer drive current	-	-	5	-	mA
Note: $T_{ambient} = 25^0$C, DVdd = 3.3 V					

Table 53. 3.3 V DC Characteristics

AC '97 2.1 ***recommends*** that new Controller and Codec designs support 3.3 V digital operation as specified in Table 53.

D.6.2 Reset

The AC '97 Architecture defines three types of reset that an AC '97 compatible Codec must comprehend:

1.	Cold reset	RESET#	complete hardware reset; all registers default state
2.	Register reset - Audio	write to 00h	all audio registers default state
	Register reset - Modem	write to 3Ch	all modem registers default state
3.	Warm reset	SYNC w/o BITCLK	re-activates AC-link; no change to register values

Registers should take their default values after Cold or Register reset, but not Warm reset. This includes all registers defined in Appendices A and B, which AC '97 2.0 erroneously specified as "default (following cold or warm reset)" instead of the correct "default (following cold or *register* reset)".

D.6.2.1 Cold Reset

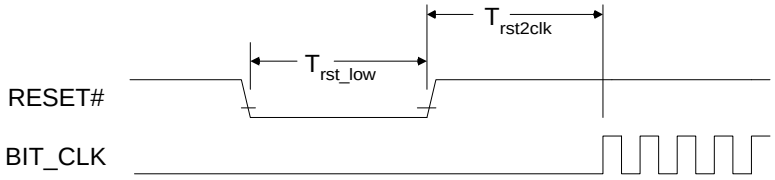


Figure 36. Cold Reset timing diagram

Parameter	Symbol	Min	Typ	Max	Units
RESET# active low pulse width	T_{rst_low}	1.0	-	-	us
RESET# inactive to BIT_CLK startup delay	$T_{rst2clk}$	162.8	-	-	ns

Table 54. Cold Reset timing parameters

D.6.2.2 Warm Reset

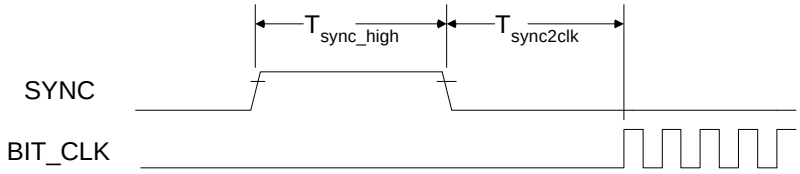


Figure 37. Warm Reset timing diagram

Parameter	Symbol	Min	Typ	Max	Units
SYNC active high pulse width	T_{sync_high}	1.0	-	-	us
SYNC inactive to BIT_CLK startup delay	$T_{sync2clk}$	162.8	-	-	ns

Table 55. Warm Reset timing parameters

The original table in AC '97 1.03 showed 1.3 us typical for SYNC high, but no minimum value corresponding to the statement made in the text: *"A warm AC '97 reset will re-activate the AC-link without altering the current AC '97 register values. A warm reset is signaled by driving SYNC high for a minimum of 1us in the absence of BIT_CLK."*

Please note that this minimum SYNC pulse width pertains to warm reset only, during normal operation SYNC is asserted for the entire tag phase (16 BIT_CLK times).

D.6.3 AC-link Clocks

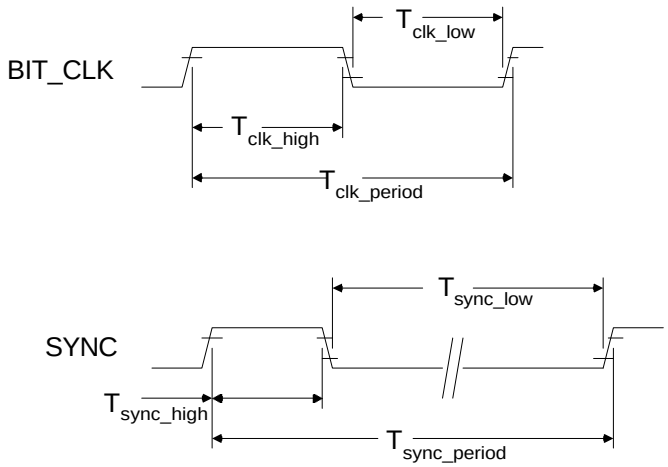


Figure 38. BIT_CLK and SYNC Timing diagram

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	T_{clk_period}	-	81.4	-	ns
BIT_CLK output jitter		-	-	750	ps
BIT_CLK high pulse width (note 2)	T_{clk_high}	36	40.7	45	ns
BIT_CLK low pulse width (note 2)	T_{clk_low}	36	40.7	45	ns
SYNC frequency		-	48.0	-	kHz
SYNC period	T_{sync_period}	-	20.8	-	us
SYNC high pulse width	T_{sync_high}	-	1.3	-	us
SYNC low pulse width	T_{sync_low}	-	19.5	-	us
Note 1: 47.5-70 pF external load as per Table 63 Note 2: Worst case duty cycle restricted to 45/55 ***(was 40/60 prior to AC '97 2.1)***					

Table 56. BIT_CLK and SYNC Timing Parameters

D.6.4 Data Output and Input Times

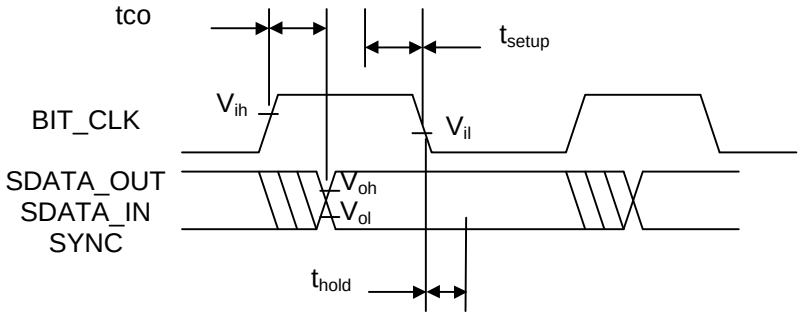


Figure 39. Data Output and Input Timing Diagram

Parameter	Symbol	Min	Typ	Max	Units
Output Valid Delay from rising edge of BIT_CLK	tco	-	-	15	ns
Note 1: Timing is for SDATA and SYNC outputs with respect to BIT_CLK *at the device driving the output* Note 2: 50 pF external load					

Table 57. AC-link Output Valid Delay Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Input Setup to falling edge of BIT_CLK	t_{setup}	10	-	-	ns
Input Hold from falling edge of BIT_CLK	t_{hold}	10	-	-	ns
Note: Timing is for SDATA and SYNC inputs with respect to BIT_CLK *at the device latching the input*					

Table 58. AC-link Input Setup and Hold Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK combined rise or fall plus flight time (Primary Codec to Controller or Secondary)		-	-	7	ns
SDATA combined rise or fall plus flight time (Output to Input)		-	-	7	ns
Note: Combined rise or fall plus flight times are provided for worst case scenario modeling purposes					

Table 59. AC-link Combined Rise or Fall plus Flight Timing Parameters

The original AC '97 1.03 specified SDATA and SYNC to BIT_CLK setup and hold times for point-to-point Controller to Codec connections. The multiple Codec configurations defined by AC '97 2.0 introduce Secondary Codecs that derive their AC-link timing from a Primary Codec's BIT_CLK. Riser solutions under development define system implementations where AC-link signal trace lengths can run up to ~15 inches, with total external capacitive loads of 50 pF or greater. Both of these can impact SDATA and SYNC to BIT_CLK timing relationships, as well as strength of the AC-link output pin drivers.

The typical Controller or Codec updates an AC-link output signal on the rising edge of BIT_CLK, drives it valid prior to BIT_CLK falling, and holds it valid for the entire duration of BIT_CLK low. The typical Controller or Codec latches AC-link input signals on the falling edge of BIT_CLK. The new Output Valid Delay timing parameters and reduced Input Setup and Hold times help guarantee AC-link operation for multiple Codec and/or riser implementations.

Rise and Fall times, flight times, Output Valid Delay, Input Setup and Hold, and worst case capacitive loads (section D.6.8 below) should be used together for modeling of the AC-link output pin drivers.

For example, the following worst case scenario situates the Primary Codec along with a Secondary Codec on a riser 15 inches from the Controller. The AC-link BIT_CLK, SYNC, and SDATA_OUT signals are loaded with ~55 pF external capacitance. The Primary drives BIT_CLK to the Controller with a 7 ns combined rise plus flight time, the Controller delays 15 ns in driving SDATA_OUT valid (includes the 7 ns return combined rise or fall plus flight time), and the Codec requires stable data 10 ns prior to latching. Assuming the minimum BIT_CLK high time of 36 ns (guaranteed by the new 45/55 duty cycle requirement) yields:

36 – (7 + 15 + 10) = 4 ns margin

D.6.5 Signal Rise and Fall Times

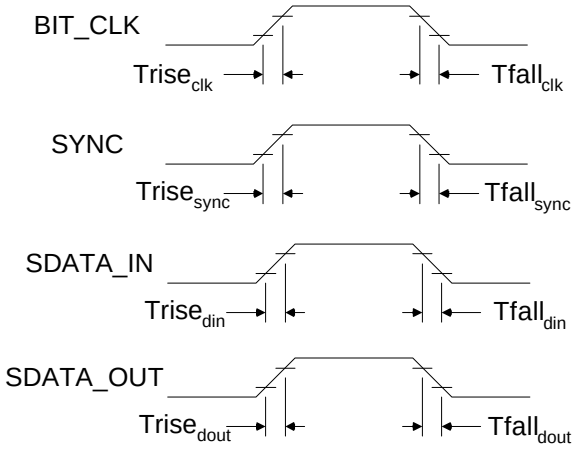


Figure 40. Signal Rise and Fall Timing Diagram

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK rise time	$Trise_{clk}$	2	-	6	ns
BIT_CLK fall time	$Tfall_{clk}$	2	-	6	ns
SYNC rise time	$Trise_{sync}$	2	-	6	ns
SYNC fall time	$Tfall_{sync}$	2	-	6	ns
SDATA_IN rise time	$Trise_{din}$	2	-	6	ns
SDATA_IN fall time	$Tfall_{din}$	2	-	6	ns
SDATA_OUT rise time	$Trise_{dout}$	2	-	6	ns
SDATA_OUT fall time	$Tfall_{dout}$	2	-	6	ns
Note 1: 50 pF external load Note 2: rise is from 10% to 90% of Vdd (V_{ol} to V_{oh}) Note 3: fall is from 90% to 10% of Vdd (V_{oh} to V_{ol})					

Table 60. Signal Rise and Fall Time Parameters

AC '97 2.1 maintains the original specified BIT_CLK, SYNC, SDATA_OUT, and SDATA_IN signal rise and fall times. These signals must also meet the new Output Valid Delay time with respect to the *rising* edge of BIT_CLK specified in Table 57.

Modeling of the AC-link output pin drivers should include rise and fall times, flight times, and external capacitive loads, which could be a large as 70 pF. Special consideration should be given to the BIT_CLK output pin driver for any Primary Codec that is designed to operate in multiple Codec and/or riser implementations.

System designers should be aware that point-to-point routings with low total capacitive loads might require EMI reduction techniques, such as series resistors.

D.6.6 AC-link Low Power Mode Timing

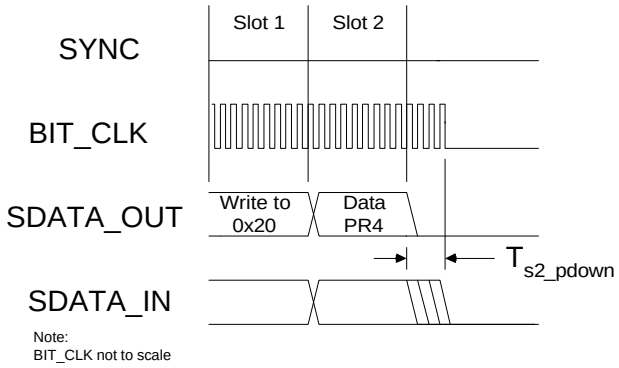


Figure 41. AC-link low power mode timing diagram

Parameter	Symbol	Min	Typ	Max	Units
End of Slot 2 to BIT_CLK, SDATA_IN low	T_{s2_pdown}	-	-	1.0	us

Table 61. AC-link low power mode timing parameters

D.6.7 ATE Test Mode

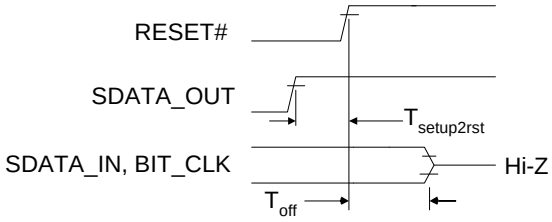


Figure 42. ATE test mode timing diagram

Parameter	Symbol	Min	Typ	Max	Units
Setup to trailing edge of RESET# (also applies to SYNC)	$T_{setup2rst}$	15.0	-	-	ns
Rising edge of RESET# to Hi-Z delay	T_{off}	-	-	25.0	ns

Table 62. ATE test mode timing parameters

Notes:
1. All AC-link signals are normally low through the trailing edge of RESET#. Bringing SDATA_OUT high for the trailing edge of RESET# causes AC '97's AC-link outputs to go high impedance which is suitable for ATE in circuit testing.
2. A vendor-specific internal test mode can be entered by bringing SYNC high for the trailing edge of RESET#. This mode has no effect on AC '97 AC-link output signal levels.
3. Once either of the two test modes has been entered, AC '97 must be issued another RESET# with all AC-link signals low to return to the normal operating mode.

D.6.8 AC-link IO Pin Capacitance and Loading

In multiple Codec implementations, the AC '97 2.1 Controller drives SYNC and SDATA_OUT to two or more destinations. The Controller's SYNC and SDATA_OUT output pin drivers need to meet AC-link timing requirements when loaded by the total capacitance on each of these outputs.

In multiple Codec implementations, the AC '97 2.1 Codec drives BIT_CLK to two or more destinations. The Codec's BIT_CLK output pin driver needs to meet AC-link timing requirements when loaded by the total capacitance on this output.

The following factors contribute to total capacitance:

- Controller or Codec *output pin* capacitance (internal device characteristic)
- Codec or Controller *input pin* capacitance (7.5 pF max per AC '97 2.1, see Table 63 below)
- Total trace length capacitance on motherboard plus riser[18] (estimated 2.5 pF per inch)
- IO connectors, such as motherboard to riser (estimated 2.5 pF)

AC '97 2.1 compliance ***recommends*** that the following Controller and Codec *input pins* have a maximum of 7.5 pF capacitance. This applies to:

- Controller BIT_CLK and SDATA_IN[0-3] inputs
- Primary and Secondary Codec SYNC and SDATA_OUT inputs
- Secondary Codec BIT_CLK input

AC '97 2.1 compliance ***recommends*** the following Controller and Codec AC-link *output pin* drivers be of sufficient strength to meet AC-link timing requirements for the following specified external[19] capacitive loads in 1-4 Codec implementations:

Output pin	**1 Codec**	**2 Codec**	**3 Codec**	**4 Codec**
Controller: SYNC, SDATA_OUT	47.5 pF	55 pF	62.5 pF	70 pF
Codec: BIT_CLK (must support ≥2 Codecs)	55	55	62.5	70
Codec: SDATA_IN (always point-to-point)	47.5	47.5	47.5	47.5
47.5 pF load comprehends 1 input, 1 connector, and ~15 inches of trace length				
55 pF load comprehends 2 inputs, 1 connector, and ~15 inches of trace length				
62.5 pF load comprehends 3 inputs, 1 connector, and ~15 inches of trace length				
70 pF load comprehends 4 inputs, 1 connector, and ~15 inches of trace length				

Table 63. AC-link pin IO driver loading

[18] Motherboard plus riser trace lengths, especially in multiple Codec implementations such as AC down (motherboard) and MC up (riser), could exceed ~15 inches, particularly in NLX form factor designs.

[19] In addition to these external capacitive loads, additional allowance must be made for the particular Controller or Codec *output pin* capacitance (internal device characteristic).